Design of Source Degenerated Cascode Dual Functionality LNA/PA for the IEEE 802.15.4 (ZigBee) Standard: Part I - New Methodology

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This article presents a new compact and comprehensive design methodology for an RF CMOS, source degenerated cascode, dual functionality, low-noise amplifier (LNA) and power amplifier (PA) for the IEEE 802.15.4 standard (commercially known as ZigBee). Due to the need to meet the far apart performance requirements of both the LNA and the PA, the proposed design methodology is based on simultaneous graphical visualization of the relationship between all relevant performance parameters and the corresponding design parameters. To demonstrate the effectiveness of the proposed methodology, a design example is presented. The simulated performance of the designed amplifier at 2.4 GHz satisfies both the requirements of the ZigBee LNA and PA with a noise figure (NF) = 1.6 dB, an input third-order intercept point (IIP3) = 6 dBm and a 1 dB compression point of -3.5 dBm. At the high input power of 0 dBm, the amplifier achieves 24 percent power added efficiency (PAE) with 8 dB gain and 22 mW power consumption.

Over the years, the design of low noise amplifiers (LNAs) in CMOS technology has attracted the attention of many researchers; see for example [1-10] and the references cited therein. This is attributed to the rapidly improving CMOS technology as a result of transistor scaling. In designing an LNA, the following should be considered: power gain, noise figure (NF), impedance matching, reverse isolation, stability, distortion and power consumption. On the other hand, the design of the power amplifier (PA) is the most challenging task in a wireless communication transceiver. This is attributed to the tradeoffs between the DC power supply voltage, output power, power efficiency and linearity; see for example [11-15] and the references cited therein. In designing a PA, the following should be considered: high transmitted power, low power consumption, power added efficiency (PAE), the nonlinear amplifier characteristics and design parameters, like the third-order input intercept point (IIP3), the carrier-to-intermodulation ratio (C/I), the input 1 dB gain compression point (P1dB) and adjacent channel power ratio (ACPR). The LNA and PA designers are, therefore, confronted by a difficult trade-off among the contrasting far-apart goals of high performance in both amplifiers. Thus, in modern wireless communication systems, these two amplifiers are

designed separately. No attempt has been reported, so far, for combining the two amplifiers into one.

In the IEEE 802.15.4 (ZigBee) standard, since the output power requirement is relatively modest, it is possible to consider the design of a single amplifier block which can act as an LNA in the receiver chain and a power amplifier PA on the transmitter side. This would reduce the power consumption, chip area and size, leading to cost savings of the transceiver that is so vital to the widespread utilization of the ZigBee standard. However, since the achievable performances of the LNA and the PA are mainly limited by the CMOS transistors parameters and operating conditions, the selection and implementation of a design methodology, leading to the solution of several design problems, is the crucial point in the design of such a dual functionality LNA/PA.

The major intention of this article is, therefore, to present a new design methodology for a dual functionality LNA/PA. The proposed design methodology is based on simultaneous 3D graphical visualization of the relationship between all relevant performance parameters and corresponding design parameters. In this regard, the intention is to generate and provide a set of design graphs that can be used by the designer. A design example is then presented to demonstrate the effectiveness of the proposed methodology and the quality of trade-offs it allows the designer to make.

Design Approaches of Inductively Degenerated Cascode LNAs

The common-source (CS), common-gate (CG) LNA topology, shown in ***Figure 1***, has been and still is by far the most common LNA topology in use; see for example [16-18]. One of the major advantages of this topology is that it allows independent optimization of noise and linearity by optimizing the CS and CG transistors separately [20-22]. Moreover, compared to the CS LNA, the drain-gate capacitance of the transistor is no longer connected between the output and the input of the LNA. Thus, reverse isolation and stability are improved. Furthermore, because the input resistance of the CG is small, the voltage gain of the CS is almost unity, assuming that the CS and CG have the same transconductance. Thus, the Miller capacitance appearing at the input of the CS, due to the drain-to-gate parasitic capacitance of the CS, will be very small. However, this topology suffers from the following disadvantages. First, its transconductance is limited by the transconductance of the CS stage only [19]. Second, the high frequency noise and gain can be significantly degraded by several parasitics at the node between the CS and the CG transistors [23].

Shaffer and Lee [1] reported a detailed examination of the inductively degenerated cascode LNA, which to date represents the most comprehensive analysis of this topology in the literature. Moreover, they proposed an optimisation strategy based on the adjustment of the gate-source overdrive voltage to achieve a suitable trade-off between noise, gain and power consumption. However, they ignored the effect of the series resistance of the gate inductance on the performance of the amplifier by assuming a high Q off-chip inductor. This later became the focus of many of the optimisation methods, which were based on circuits adopting integrated gate inductors; see for example [24-26]. The influence of an integrated gate inductance with low Q is particularly important at high frequencies, as the loss due to its parasitic resistance increases, thus contributing to an increased noise figure [27]. In these works, the analysis is commonly

centered on the relationship between the achievable noise figure, gain and current consumption with circuit elements at the input of the amplifier including, in addition to L_G and its series resistance, the transistor width, its C_{GS}, and the degeneration inductance, L_S The basis of this comes from results reported in [28]. Under power matched conditions at the operating frequency, with the input reactance equal to zero while the input resistance equals the source resistance (R_S), the inductances L_S and L_G can be determined using Equations 1 and 2 [28].

$$L_s = \frac{(R_s - R_g)C_{gs}}{g_m} \tag{1}$$

$$L_g = \frac{1}{\omega_o^2 C_{gs}} - L_s \tag{2}$$

Where:

G_m = the transconductance of the transistor M_1 and

ω_0 = the operating frequency.

Inspection of Equations 1 and 2 reveals a trade-off challenge arising from the fact that in order to reduce L_G (hence reducing its parasitic resistance), C_{GS} has to be increased and because it can only be increased by increasing the width of the transistor, the current consumption will increase along with the transistor gain.

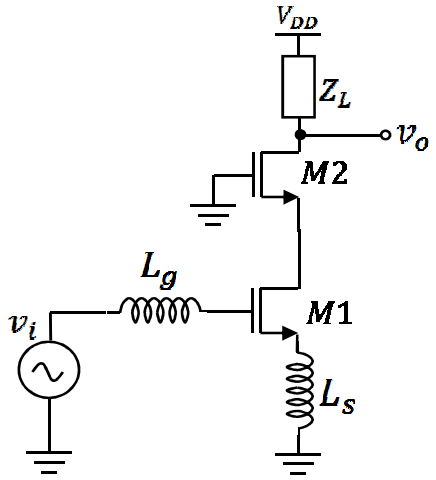


Fig. 1 The common-source common-gate cascode LNA topology

Guo and Huang [20], studied the simultaneous optimisation of noise and linearity in a cascode LNA. The noise was analysed using a cascoded noise model for the two transistors in the architecture. This study, however, was based on the Taylor series expansion, which only takes into consideration the transconductance nonlinearity of the transistors. But a more serious deficiency of this work is that the simulation carried out to assess the theoretical results only analysed the noise and IIP3 performance, subject to the gate widths of the two devices. No consideration or mention was given to the

current and the gate overdrive present at each transistor, which, as will be seen later, has a great effect on both noise and nonlinear performance, and indeed the power consumption.

Park et al [21] proposed a different approach to the simultaneous noise and linearity optimisation. This approach was based on optimising the CS stage for noise performance and the CG stage for linearity, but separately. The design was carried out by selecting a suitable gate voltage for the CS stage to constrain the current and then finding the optimum transistor size for noise performance. Separately, the IIP3 of differently sized transistors for a range of gate voltages for the CG stage was studied. The problem with this approach is that it fails to take into account the cross-dependency of the two stages. For instance, the voltage at the node between the two stages will be influenced by the bias conditions in each stage, and this will affect the noise performance separately optimised at the CS stage and the nonlinearity separately optimised at the CG stage. Moreover, although there is overwhelming dominance of the CS transistor in controlling the DC current of the cascode, there are regions, as will be seen later, where the effect of CG cannot be ignored. Having that, guaranteeing that the amplifier will perform as expected when the two separately-optimised stages are cascoded will either be impossible or will involve performing many iterations back and forth between the two separate optimisations of the first and second stage [29].

Linearization of Low-Power LNA

A MOSFET can be linearized by biasing at a gate-to-source voltage (V_{GS}) at which the third-order derivative of its DC transfer characteristic is zero [30, 31]. However, this technique is very sensitive to the bias voltage V_{GS}, as IIP3 will peak only in a very narrow range of the bias voltage. The derivative superposition (DS) method was, therefore, proposed in [32] to reduce the sensitivity of IIP3 to the bias voltage V_{GS}. In this technique, a number of parallel MOSFETs of different widths and gate biases are used to achieve a composite DC transfer characteristic with an extended range of V_{GS}, where the third-order derivative is close to zero. This technique is sometimes referred to as multi-gate transistor (MGTR) linearization. On the other hand, adaptive biasing (or dynamic bias modulation) has been suggested to increase the dynamic range of the amplifier. In this technique, the output signal is rectified and the result is used to adjust the bias such that the bias level is tuned in order for the amplifier to achieve high efficiency over a wider range of input powers [33]. Finally, it is not just the bias level that has an impact on linearity but the choice of the bias network as well. For instance, a current-derived bias results in less IIP3 variations from part to part than a voltage-derived bias [34].

On the other hand, source and load terminations are very critical in determining the nonlinear performance of an amplifier. At the output, the output matching network determines the amount of power delivered to the load; a better matching network delivers more power to the load, hence increasing the efficiency of the amplifier. Also, since the gain of the amplifier is dependant on its load impedance, the point at which the gain compresses is also dependant on the output termination, which determines the load impedance seen by the active device. Matching impedances also affect the resultant IIP3 and other intercept points of the amplifier [35]. Moreover, different matching networks have varying responses to different frequency components. For instance, if the output

matching network at the load had a terminating response to the third-order intermodulation distortion frequency, a considerable magnitude of the IM3 product may be attenuated before it reaches the load, leading to an increase in IIP3. Also, an input matching network that was designed for optimum noise performance at the source, for instance, may have a frequency response to the second harmonic component that terminates this frequency, thus avoiding its feedback to the input leading to IIP3 improvement. Out-of-band harmonic termination can also help in improving the linearity of the LNA [36]. Volterra series analysis was used to find expressions for the third-order intermodulation component (IMD3) and the third-order intercept point (IIP3) of a common-emitter bipolar junction transistor (BJT). By adapting these equations for a CS MOSFET, these equations have emerged to be the basis of a significant portion of linearization concepts proposed in recent times [37, 38]. The results reported in [48] show that the improvements in IIP3 and IMD3 that can be achieved in a MGTR and second-harmonic terminated amplifier are much greater than in a MGTR only amplifier. However, according to [34] the use of the MGTR technique may degrade the noise figure. Modified versions of the MGTR technique have been reported in [39, 40]. Furthermore, the termination of the second harmonic component can also help improve efficiency [41]. This is because this frequency component can change the shape of the drain current waveform and thus affect the power consumption. In general, the efficiency of power amplifiers can be improved by providing proper terminations at harmonic frequencies for both load and source [42-44]. For low power operation the optimum source and load terminations can be found using techniques such as gain and noise circles [56], while for high power operation, optimum source and load terminations are determined by carrying out a simulation-based source-pull and load-pull investigation [45].

Limitations of Current Design Approaches

In addition to the limitation of separately optimising the CS and CG stages, which often requires repeated iterations in the design process, there are three limiting factors that are common between all the design approaches discussed in the previous sections. These can be summarised as follows:

1. They are all based on theoretical mathematical expression-based modelling of the devices used and the circuit topologies. This approach is not conclusive, for a number of reasons. First, the theoretical mathematical expression-based analysis often involves several assumptions to both simplify the models by ignoring supposedly insignificant parasitics; see for example [24, 46, 47] or simplification of the equations by removing supposedly insignificant terms; see for example the design methods in [26, 48-53]. While such steps may be necessary since manipulation can be impossible if the full models and equations are considered, the insignificancy judgement is left to the designer and hence is very variable and can be unreliable. This reduces the accuracy of the results obtained with the mathematical-based design methodologies [54]. Second, the modelling equations often have a narrow spectrum, meaning, although they show how parameters are related, they are difficult to interpret in terms of how this relationship will change if one of the parameters was confined to certain value limits. This reduces the amount of information that the design approach can give, and can lead to an incorrect identification of the starting point.

2. Because of the limited scope of the mathematical equations, most of these mathematical expression-based design optimisation methods lead to only a starting point for each design parameter. Designers then have to run an automatic optimisation routine in a commercial simulator, specifying performance requirements and letting the simulator find the ultimate optimum point; see for example [55-57]. But this can lead to inaccuracies since, in addition to the possibility that the starting point resulting from the simplified mathematical equations is not accurate, the optimiser, which is itself based on mathematical methods, might not be able to find the optimum solution starting from the initial point with the number of iterations specified. Increasing the number of iterations requires more memory power and can be very time consuming, adding pressure on time-to-market demands.

3. Finally, but most importantly, in these design approaches, the designer will not be made aware of what performance parameters were traded in the "optimisation" and therefore cannot make a quick decision on how to make amendments to the design to change its performance if needed. This reduces the flexibility of the design method.

Proposed Design Methodology

An optimal design methodology is one that would simultaneously consider all performance requirements against all design parameters. But as the functional requirements of the circuit under design and the number of components involved increase, this becomes increasingly difficult to attain. Instead, increasing knowledge of how circuit elements operate and the significance of the influence certain design parameters have on certain performance parameters can facilitate a design approach where effective early eliminations can be made, leading to as many performance parameters as possible being considered simultaneously against a limited number of design parameters. The design methodology proposed here is built around this course of action. The representation is based on visual observation, in 3D graphs, of how performance parameters vary with related design parameters, taking into account the multiple dependencies of performance parameters on design parameters. Components are simulated between their minimum and maximum values to explore their full potential and uncover areas of their operation where better results may be obtained. After some initial eliminations and considerations, most of the performance parameters are simulated with respect to the same design parameters. This allows the designer to simultaneously analyse the effect of these design parameters on all those performance parameters and hence make satisfactory trade-off decisions. This also gives the designer the ability to reuse the results of this analysis and change trade-off choices if another design with different constraints is needed.

The proposed design procedure of the dual functionality LNA/PA is based on optimising the two stages of the cascode architecture to simultaneously meet the requirements of low-noise operation at higher than usual input powers. This approach reduces the need for iterations in later stages of the design flow as has been the case with some of the works reviewed in previous sections. All analysis, optimisation and design work presented in this section were carried out using components from a 0.18 μm RFCMOS mixed signal design kit from United Microelectronics Corporation (UMC). This is the design kit with the smallest available CMOS transistors compatible with the advanced design system (ADS) software. The proposed design methodology is

divided into three main steps: the optimisation of the core circuit components (including bias voltages); the addition and optimisation of linearization techniques; and the optimisation of input and output matching networks.

Optimisation of the Core Circuit Components

The core amplifier circuit (that is excluding the matching) to be optimised in this work is shown in ***Figure 2***. It includes the two cascode transistors and the load inductance. The optimisation procedures described here assumes that the inductors of the cascode architecture will only insignificantly affect the DC characteristics of the amplifier due to their relatively small internal resistances. Therefore, the DC analysis can safely be done on the two cascode transistors only without including the inductors, and the results will still be valid when the inductors are connected. Moreover, due to the limited range of values of inductors that are commonly considered for use either as a degeneration inductance in the source of the CS stage or as a load inductance in the drain of the CG stage, a compromised configuration (bias point and device width) for the cascode transistors produced from analysis of the circuit without inductors will not be much different if the analysis was undertaken with the existence of the inductors.

The first step in optimising circuit components is to tune the sizes and biases of the two cascode transistors, without the inductive degeneration.

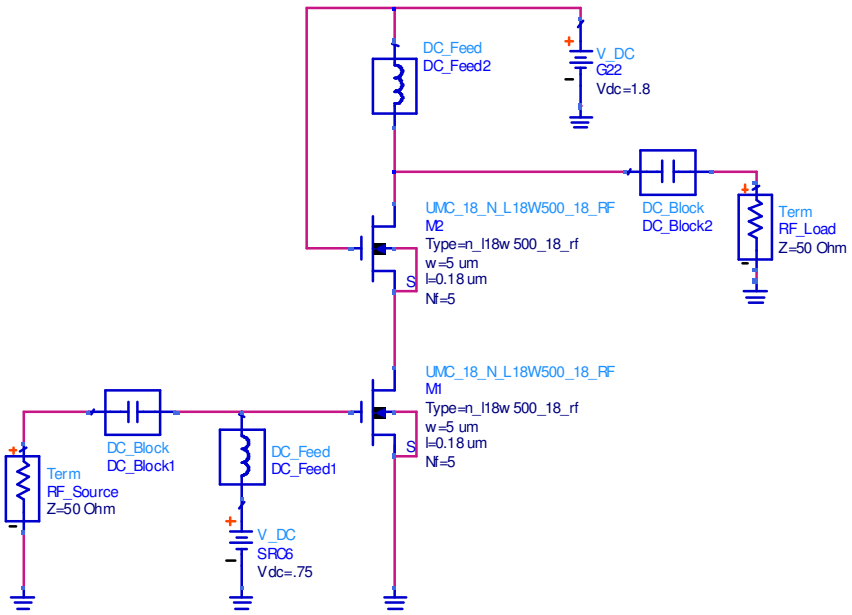


Fig. 2. Initial optimisation circuit for the two cascode transistors without the inductive degeneration

The general approach is to examine all the low and high-power performance parameters concerned, against a sweep of sizes of the CS and CG transistors, after appropriately setting the bias voltages at the gates of each stage. In the figure, the gate of the CG transistor is connected to the DC supply voltage V_{DD}. This choice is motivated by consideration of Equation 1 [50].

$$IIP_{3_2} = \frac{4}{3}\left|\frac{V_{GS_2}(2+\theta V_{GS_2})(1+\theta V_{GS_2})}{\theta}\right| \quad (3)$$

In Equation 3, IIP3 is the input referred third-order intercept point of transistor M2, V_{GS} and θ are the DC gate-to-source voltage and the normal field mobility degradation factor of M2. Equation 3 suggests that the IIP3 can be enhanced by increasing V_{GS}. Hence, to increase the flexibility and reduce the scope of possibilities, it is proposed to connect the gate of M2 to the DC supply voltage V_{DD}. Thus, V_{GS} will be decided by the voltage at the node between the two transistors, hereafter called the "mid-voltage". The RF choke placed on the drain of the CG transistor isolates the DC supply voltage from the amplifier RF output. The bias voltage and the size of the CS transistor, the dominant contributor to noise in the amplifier, are adjusted with respect to its noise performance. The most suitable CS gate voltage, resulting from a comprehensive DC analysis of the cascode architecture, will be used as a fixed value for the rest of the optimization process. Power, gain and nonlinear analysis will be performed by investigating the effect of varying the sizes of the CS and CG transistors on several performance parameters at low and high input powers.

The second step in setting the core circuit components is to include the degeneration inductance and study its effect on both the low power and high power operation. The degeneration inductance affects low power operation in terms of noise for the LNA functionality and affects the nonlinear performance since it is classified as a negative feedback element. The final step in setting the core circuit parameters is performed by tuning the load inductor. This step is carried out after the transistor sizes and the degenerating inductor have been chosen. The load inductor has a considerable effect on two performance parameters; power gain and stability. The stability of the final amplifier circuit will depend on the impedances presented to the amplifier at the input and the output. In the best case, the core amplifier circuit (before matching) should present unconditional stability. This gives the designer more flexibility in matching the circuit for other performance parameters such as noise, gain and harmonic termination. However, trying to peruse this goal at the beginning of the design flow will significantly complicate the design process, add to design time and may result in unnecessary constraints on other desired performance parameters. Instead, this step is left as the last step in the design of the core amplifier and the value of the inductor can be decided as a simple trade-off of how it affects stability and gain only.

In the proposed design methodology, the linearization of the cascode will be performed by MGTR and harmonic termination techniques. The auxiliary transistors for MGTR linearization will be added after finalizing sizes and biases of the main transistors. This is because the bias and width of the auxiliary transistors are adjusted to cancel the third-order nonlinearity in the transconductance of the main transistor. Thus, their configuration will not be effective if the configuration of the main transistor is changed. Thus, first the width of the main transistors will be decided, based on the various amplifier performance parameters such as noise, gain and PAE and second the transistors will be linearized by the MGTR. Since it does not significantly affect the DC current in the cascode, adding auxiliary MGTR will not affect any other performance parameters set by optimizing the main transistors but will only improve its linearity. Linearization by MGTR will still be valid at relatively high powers because although the instantaneous transconductance g_m will change with high powers, the average value will remain almost constant. The harmonic termination will be incorporated within the

source- and load-pull analysis which will be extensively extended to take into account all possible terminations. Any impedance representing considerable termination to any frequency component which contributes to the third-order intermodulation distortion (IMD3) will be reflected in the input and output contours and can then be picked by the designer for matching. Matching the amplifier will be the last step in this design methodology. In high power operation, matching techniques based on the S-parameters, which is essentially a small signal analysis, cannot be used. Instead, source and load pull simulations will be used by considering a number of different matching impedances spread across the Smith chart and investigate the response of the circuit in terms of obtainable performance parameters when these impedances are presented to the input and the output of the core amplifier circuit, respectively.

DC Analysis of the Core Circuit

In this section, the DC current and DC voltage of the cascode architecture are analysed based on the circuit shown previously. The analysis is performed over a range of sizes of the CS and CG transistors. ***Figures 3*** and ***4*** show how the DC current and the DC voltage at the mid point between the two stages vary with respect to different combinations of sizes of the two transistors, at several DC supply voltages (voltage at the drain of the CG transistor). CS NGF is the number of gate fingers of the CS transistor and CG NGF is the number of gate fingers of the CG transistor, each gate finger is 5 µm wide.

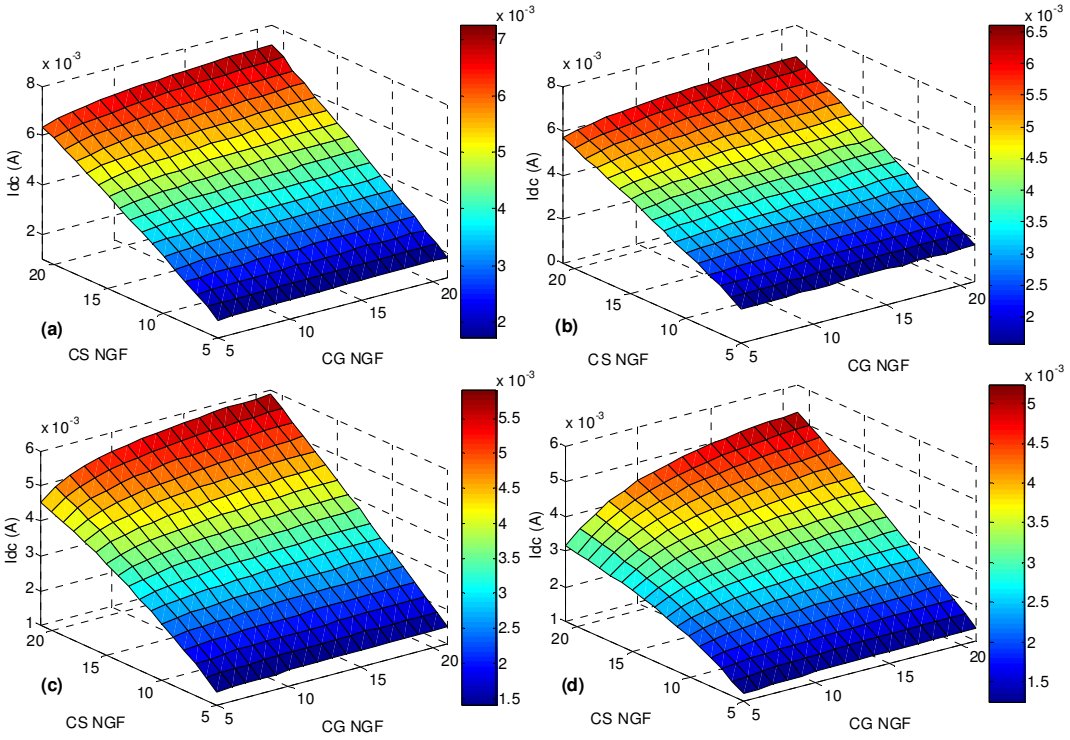


Figure 3. Amplifier DC current versus CS and CG sizes at DC supply voltage of (a) 1.8V, (b) 1.5V, (c) 1.2V and (d) 1.0V

Figure 3 clearly indicates a higher dependence of the DC current on the size of the CS transistor than on the size of the CG transistor. This is because the gate-to-source voltage of the CS transistor is fixed, unlike the V_{GS} of the CG transistor. As from Figure 2, because the voltage at the gate of the CG transistor is fixed and since the voltage on

its source is the mid-voltage, its V_{GS} changes every time the sizes of the transistors change. In this sense, the CS transistor acts as a current source, the current of which depends on its size and gate voltage. The CG transistor absorbs that current and the only change it observes is the distribution of that current beneath each of its gate fingers, but the total current generally does not change as a result of changing the size of the CG transistor.

An important observation to note from Figure 3 is that the dependence of the DC current on the size of the CG transistor changes as the supply voltage varies. As shown in Figure 3, this dependence increases at smaller sizes of CG transistor as the supply voltage drops when the CS transistor is large. This can be explained as follows: when the size of the CS transistor is increased, it demands more current, and since the two transistors are cascoded, this current has to be passed through the CG transistor. At higher values of DC supply voltage, the CG transistor does that by changing its overdrive voltage. This is evident from Figure 4(a); the mid-voltage decreases as the size of the CS transistor increases, hence increasing V_{GS} of the CG transistor, facilitating the current increase. However, Figure 4 shows that as the CG transistor size decreases, the mid-voltage decreases. This affects the current on two fronts: First, since the decrease in the mid- voltage is not proportional to the decrease in the supply voltage, the CG transistor can no longer attain high V_{GS} at lower supply voltages as it does when the supply voltage is high. Second, the mid-voltage may be reduced to a level effectively taking the CS device out of its saturation region. When the CS transistor is in the linear region, the current it tries to draw decreases and the more the CG transistor size is reduced (when CS transistor is large), the more the mid-voltage is reduced and hence the CS transistor is pushed further away from saturation. These two notions explain the increased dependence of the DC current on the CG transistor size at lower supply voltages. Note that this observation was only possible to be made as a result of this unique 3D graphical representation of the current changes; an insight that would be very hard to acquire by studying model equations describing the DC current in the cascode configuration alone.

Figure 4 is also useful in guiding the designer on how the sizes of the CS and CG transistors might affect their areas of operation taking them between the linear and saturation regions. The CG transistor will always be in saturation since the DC voltage on its gate is the same as that on its drain. This means that, with any voltage at its source (the amplifier mid-voltage), its V_{DS} is always going to be larger than $V_{GS} - V_T$. For the CS transistor, however, the situation is different. If the DC voltage on its gate is set for example to 0.75 V, Figure 4(d) shows that when the DC supply voltage is set to 1V, there is a range of CS and CG sizes that is going to take the CS transistor out of saturation. The same applies to Fig. 4(c), but as the DC supply voltage increases to 1.2 V, the range of sizes taking the CS transistor out of saturation decreases. It can also be observed from Figure 4 that the mid-voltage is highest when the CS transistor is very small and the CG transistor is very large, this is because, in this case, the effective resistance of the CS transistor is at its highest while the effective resistance of the CG transistor is at its lowest, and therefore there is more voltage drop on the CS transistor than on the CG transistor. Opposite analysis explains why the mid-voltage is at its lowest when the CS transistor is at its largest size and the CG transistor is at its smallest size.

Since the DC current in the cascode is largely more dependant on the CS transistor rather than the CG transistor, as explained above, it is useful to study how this

current is affected by both the size of the CS transistor and its gate voltage. ***Figure 5*** presents this relationship. As shown, the DC current in the CS transistor is equally dependant on its gate voltage and size for the span simulated, which is the maximum span for the transistor size and the maximum realistic (for low power operation) span of the gate voltage. This feature will be useful in taking design decisions at later stages of the design flow.

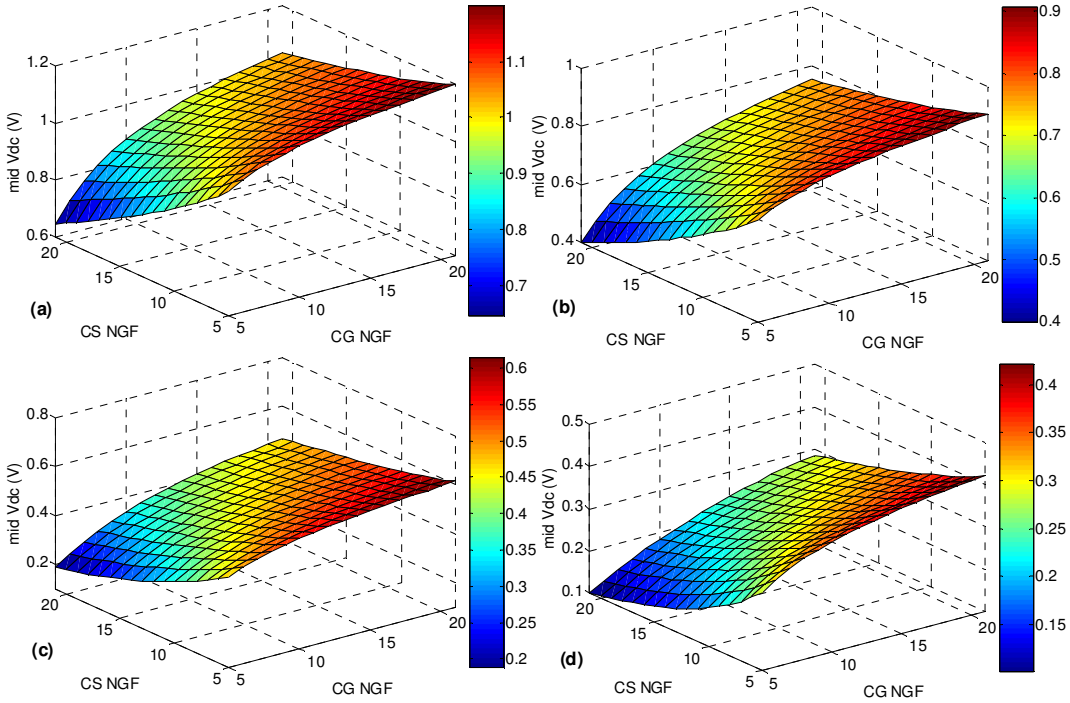


Figure 4. Amplifier mid-voltage at a voltage supply of: (a) 1.8V, (b) 1.5V, (c) 1.2V and (d) 1.0V

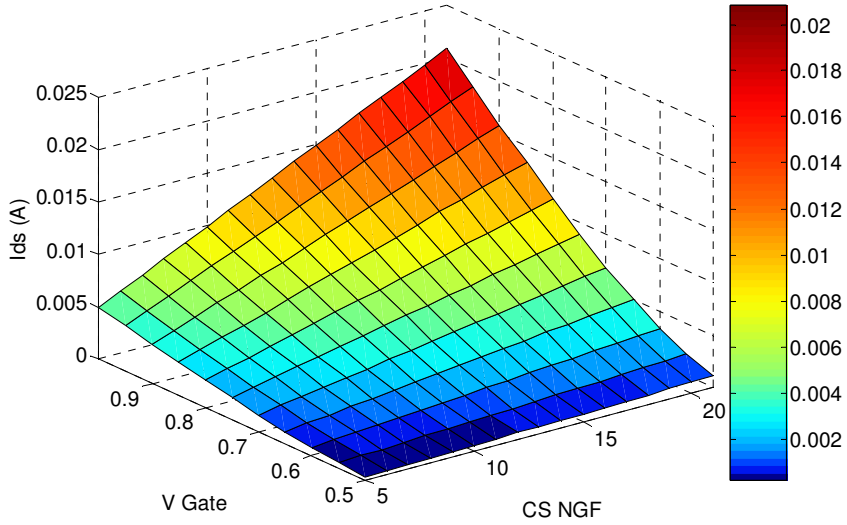


Figure 5. Common-source transistor's current versus its size and gate voltage

Noise Analysis of the Cascode Architecture

Figure 6 shows how the minimum noise figure (NF_{min}) changes with respect to different combinations of sizes of the CS and CG transistors. This graphical representation of the relationship generally agrees with the mathematical equation-based conclusions of [20] and [21] that the noise figure is almost independent of the size of the CG transistor. However, because this graphical representation is more comprehensive, it shows that this general conclusion starts to become questionable when the size of the CS transistor is significantly larger than that of the CG transistor. The reason for this can be extracted from the DC analysis as follows: At larger sizes of the CS transistor, and as the size of the CG transistor decreases, both the total current and the mid-voltage decrease. This means that the CS transistor is retreating from its relatively high gain operation region to its linear region, inevitably increasing the minimum obtainable noise figure.

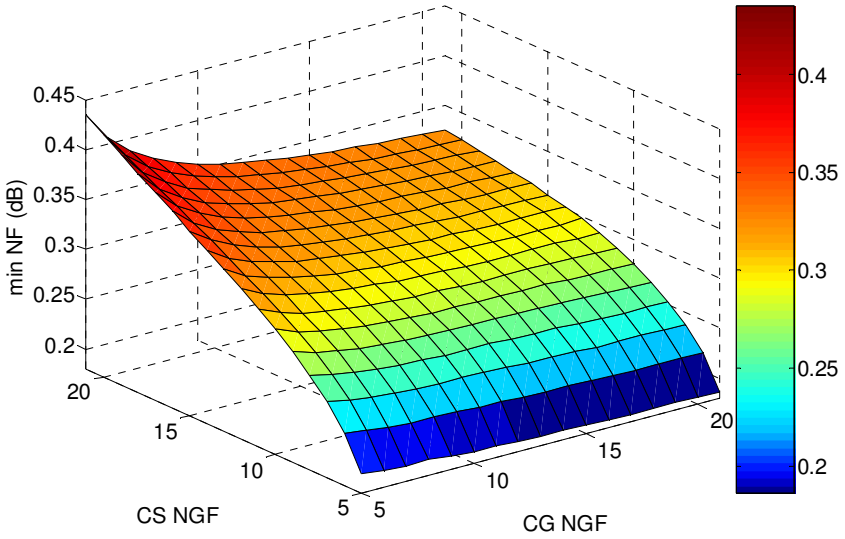


Figure 6 Minimum noise figure versus transistor sizes

Based on the results shown, and given that it is very unlikely for the size of the CS device to be chosen less than 50 μm (since this will mean very small current and insufficient gain), it follows that it is safe to optimise the noise performance of the cascode by considering the noise performance of the CS transistor alone, as long as the fact that the bias condition of the CG transistor will affect the voltage on the drain of the CS transistor is taken into consideration. This implies that the CS transistor noise analysis has to be repeated for a range of possible values of mid-voltage generated in Figure 4. The voltage on the drain of the CS transistor is important because it will affect the current through it and hence the noise. Therefore, in order to take into account the three parameters of the CS transistor that affect its noise performance (its size, gate and drain voltages) the minimum noise figure is simulated with respect to the gate voltage for different transistor sizes, and this simulation is then repeated for several drain voltages. The results of these simulations are presented in the 3D graphs of ***Figure 7***. It presents an interesting and very useful result showing that there is a persistent reduction in the minimum noise figure at gate voltage in the vicinity of 0.75 V and that is maintained for all sizes of transistor and at all drain voltages. It also shows that the

noise figure generally decreases as the supply voltage on the drain of the common-source transistor increases, which agrees with the conclusions of [58].

Power and Gain Analysis of the Cascode Architecture

In this section, the influence of varying the sizes of the two transistors in the cascode architecture on power consumption, gain, and PAE is analysed. The analysis is performed by simulation for the various parameters at different input powers to examine the effect on the performance of the amplifier in low and high power regimes of operation. ***Figure 8*** shows how the DC current drawn from the DC supply changes as the transistor sizes are varied, and at different input powers.

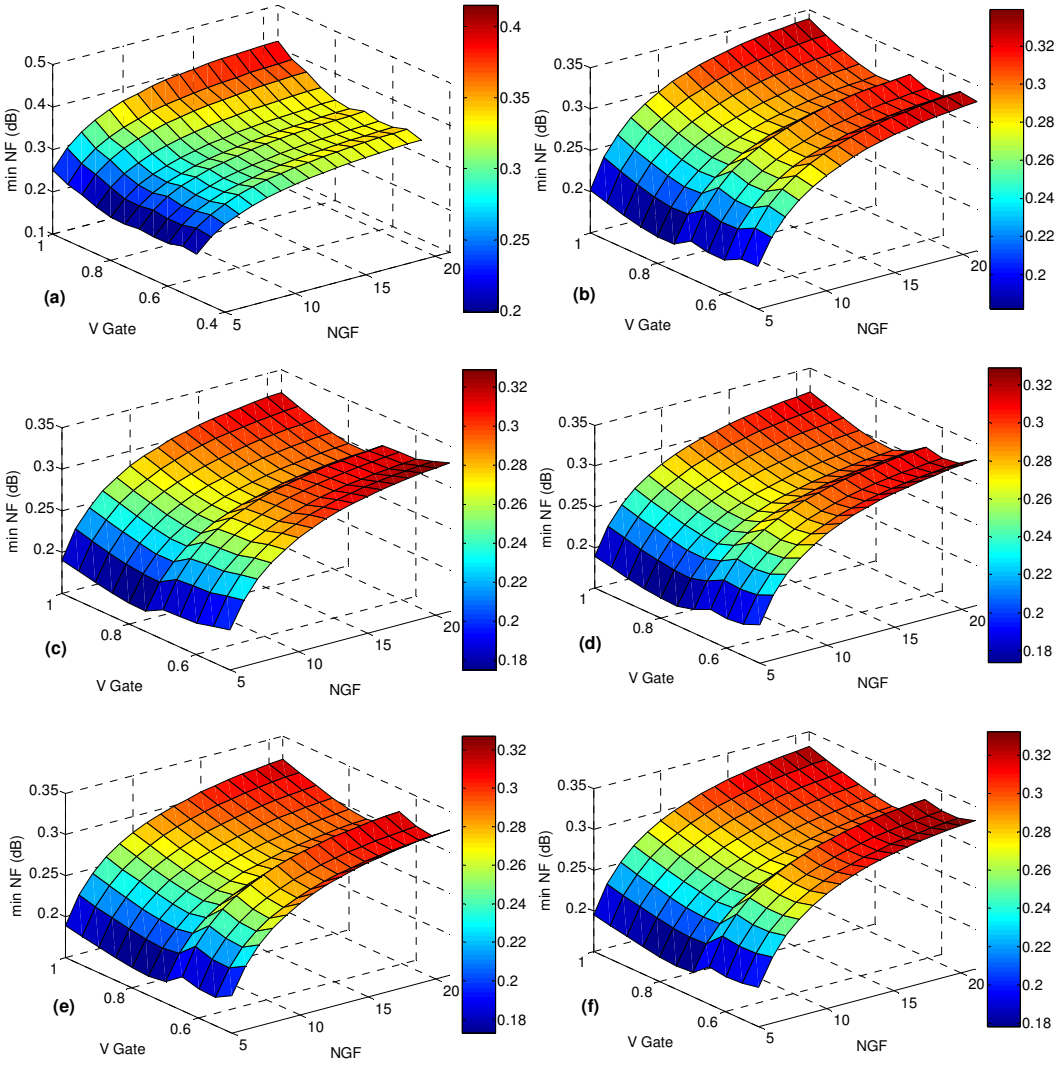


Figure 7 Minimum noise figure of a common-source transistor versus its gate voltage and size at drain voltages of: (a) 0.3V, (b) 0.5V, (c) 0.9V, (d) 1.2V, (e) 1.5V and (f) 1.8V

From Figure 8, it appears that there is no noticeable difference between Figure 3(a) and Figure 8(a), that is, the low power operation does not change the DC power characteristic from the DC analysis. However, by inspecting the graphs in Figures 8(b),(c),(d) and comparing with Figure 8(a), an interesting observation can be made. That is, in the low power regime, the current is more influenced by the size of the CS transistor than the CG transistor, but as the input power increases, an extended dependency on the size of the CG transistor is introduced. In fact, when the CG transistor is small, that is its transconductance is small and does not dominate the overall performance, the DC current is the same at all levels of input powers. But at higher input powers, and as the size of the CG transistor increases, the current drawn from the DC supply starts to increase. The justification of this phenomenon can be related to nonlinearity since as the input power increases, the two transistors are pushed more into their non linear regions. But the fact that the increase in DC current at high powers comes as the size of the CG transistor becomes larger means that the nonlinearities (in this case the even-order nonlinearities which

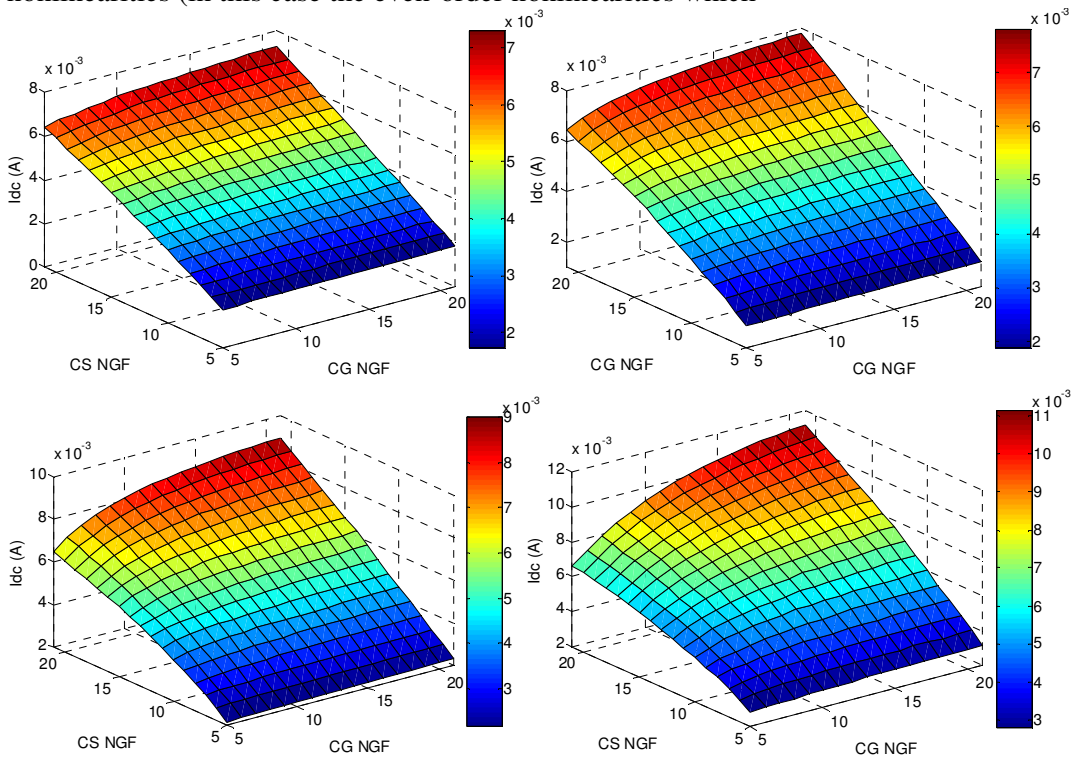


Figure 8. The DC current of the amplifier drawn from the supply at an input power of (a) -20 dBm and (b) -10 dBm (c) -5 dBm and (d) 0 dBm

produce the DC components) are produced more from the CG transistor than from the CS transistor and hence the CG transistor dominates the nonlinear performance. This result generally agrees with the conclusions of [20] and [21], which were based on mathematical equations, but further gives a visual presentation of the extent of the effect.

Figure 9 shows how the DC power consumption changes with respect to varying transistor sizes at different input powers. As expected, there is a direct relationship between the DC current and the DC power consumption. Nevertheless, this

graph is important as it informs the designer on the expected DC power consumption for given transistor sizes.

Figures 10 to ***12***, relate the gain, power delivered to the load, and PAE to the CS and CG transistor widths. These figures show that all these performance parameters merely depend on the current in the cascode. These graphs can be used simultaneously by the designer to make trade-off decisions when choosing the transistor sizes.

It is important to emphasise that these results present grounds for comparison on which the designer can make early trade-off decisions but are not definitive final results of the amplifier. This is because, particularly with the dual functionality amplifier intended in this article, trade-off decisions on the matching conditions of the amplifier are yet to be made.

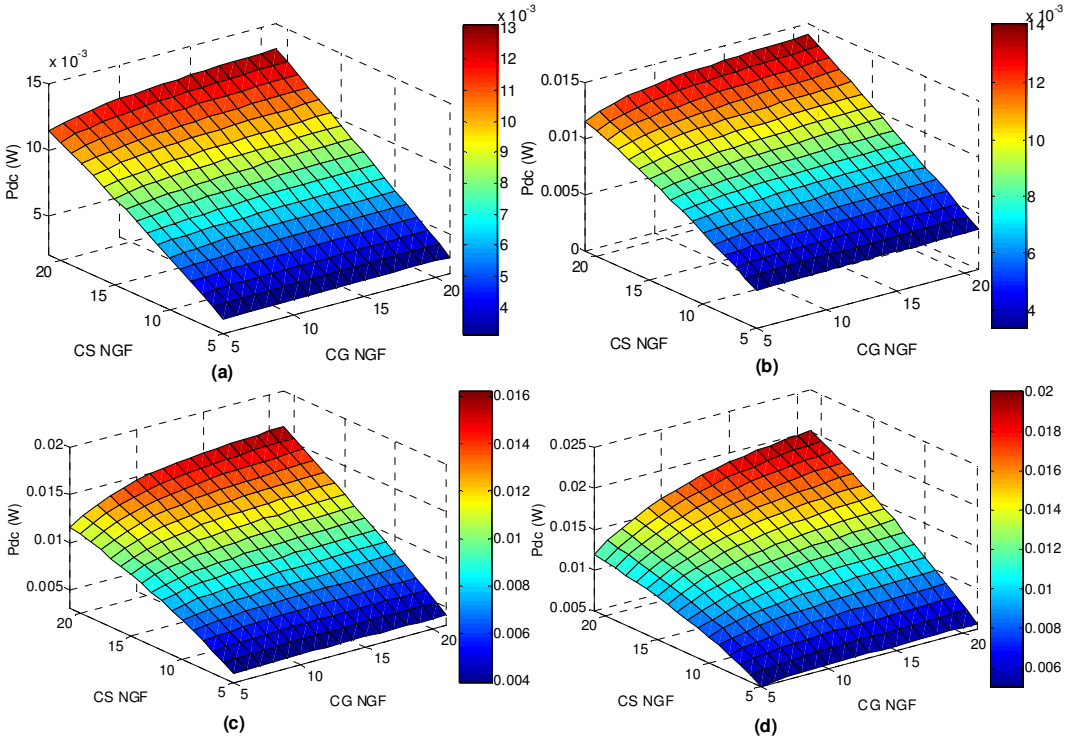


Figure 9 DC power consumption versus transistor sizes at low and high input powers (a) -20 dBm and (b) -10 dBm (c) -5 dBm and (d) 0 dBm

Nonlinear Analysis of the Cascode Architecture

The nonlinear behaviour of the cascode architecture is studied by analysing how the relative third-order intermodulation distortion IMD3 varies when the sizes of the CS and CG transistors are varied. Frequency separation between the two input tones in this two-tone test was set to 5 MHz, which is the frequency separation between any two channels in the 2.4 GHz ZigBee band. Figure 13 shows in 3D graphs how the IMD_3

changes with respect to the sizes of the CS and CG transistors, at the low and high power operation regimes.

Figure 13 demonstrates the extent to which the CG transistor dominates the nonlinear performance in the cascode architecture. In Figure 13(a), with the input power at -20 dBm, it can be seen that when the CG transistor is large (CG NGF>13) there is almost no effect from the change in its size on the relative IMD3, and that is true for all sizes of the CS device. Outside this region (13>CG NGF>5) the effect of the CG transistor size on the IMD3 is larger than that of the CS transistor. This is noted by observing the change in IMD3 relative to 1 unit size up or down of both transistors. This observation is manifested more at larger sizes of the CS transistor and starts to become untrue as the CS transistor becomes smaller.

Therefore, a conclusion can be drawn from Fig. 13(a) that, when operating at small input powers, the effect of the CG transistor size on IMD3 increases as the size of the CS transistor increases. This is another phenomenon that demonstrates the advantage of this design methodology which is based on 3D visualisation of parameter variations.

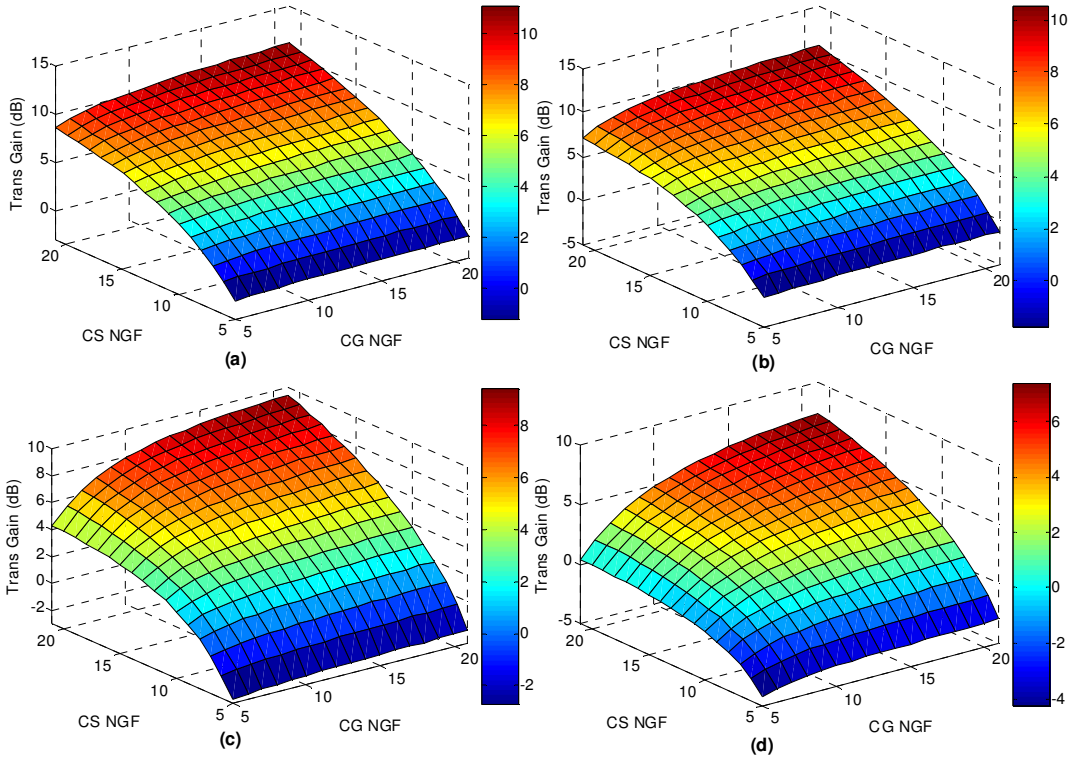


Figure 10 Transducer gain versus transistor sizes at low and high RF input powers (a) -20 dBm and (b) -10 dBm (c) -5 dBm and (d) 0 dBm

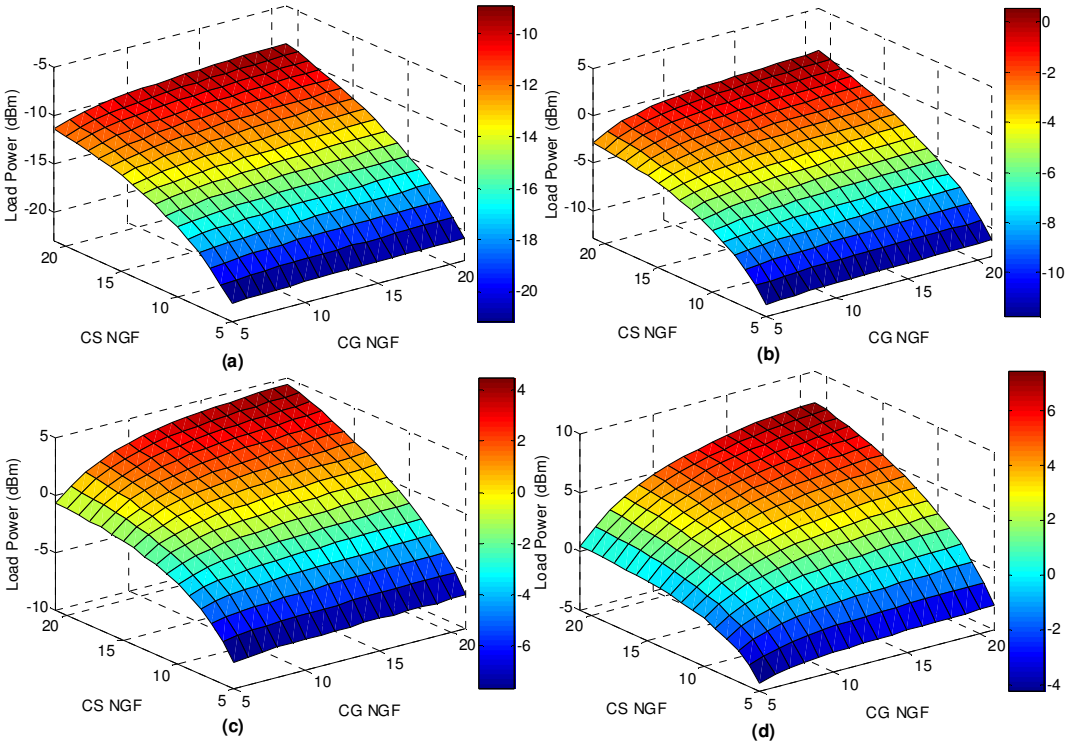


Figure 11. Load Power versus transistor sizes at low and high RF input powers:
(a) -20 dBm and (b) -10 dBm (c) -5 dBm and (d) 0 dBm

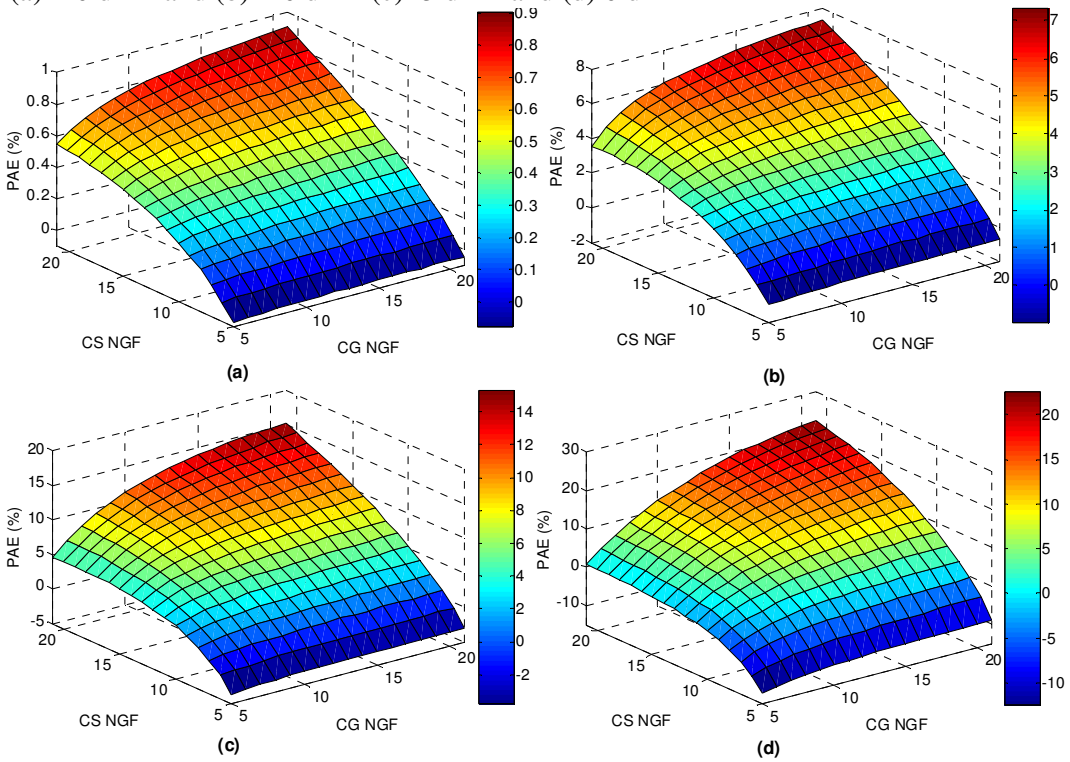


Figure 12 PAE versus transistor sizes at low and high RF input powers:

(a) -20 dBm (b) -10 dBm (c) -5 dBm (d) 0 dBm

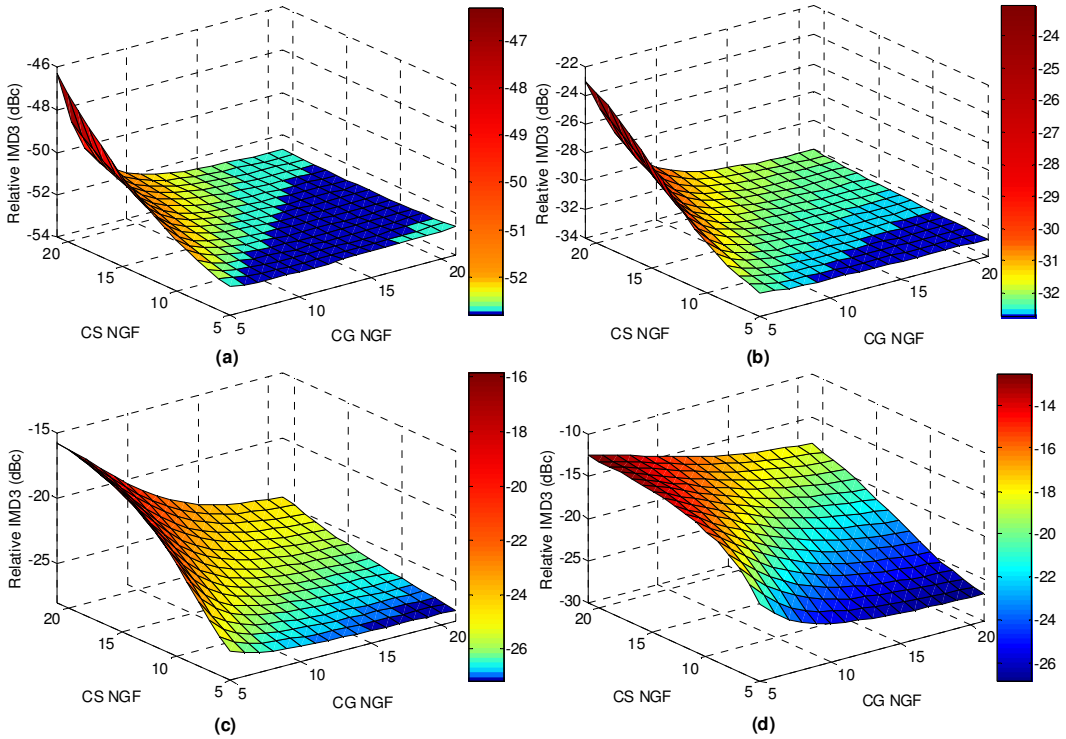


Figure 13 Variation of IMD3 in dBc with respect to transistor sizes when the RF input power is: (a) -20 dBm (b) -10dBm (c) -5dBm (d) 0dBm

It can be explained by the fact that when the CS transistor, and hence its transconductance are large, it delivers a larger signal to the CG transistor, driving it more into the nonlinear region, and hence the nonlinearities of the CG transistor are more apparent.

The observation drawn from Figure 13(a) is still true in Figure 13(b), when the input power is increased to -10 dBm. However, it can be observed that when the CS transistor is large, the range where the change in CG transistor size has no effect on IMD3 starts to decrease. In Figure 13(c), when the input power is increased to -5 dBm, this range becomes minimal and in Figure 13(d), when the input power is 0 dBm, it becomes non existent. It is also observed that with the 0 dBm input power in Figure 13(d), the effect of the CG transistor size on IMD3 is no longer dependant on the CS transistor size. This is because this input power is already very large, and irrespective of whether the CS transistor amplifies the input signal significantly or not, both transistors are driven well into their nonlinear regions and their effect on IMD3 is almost identical.

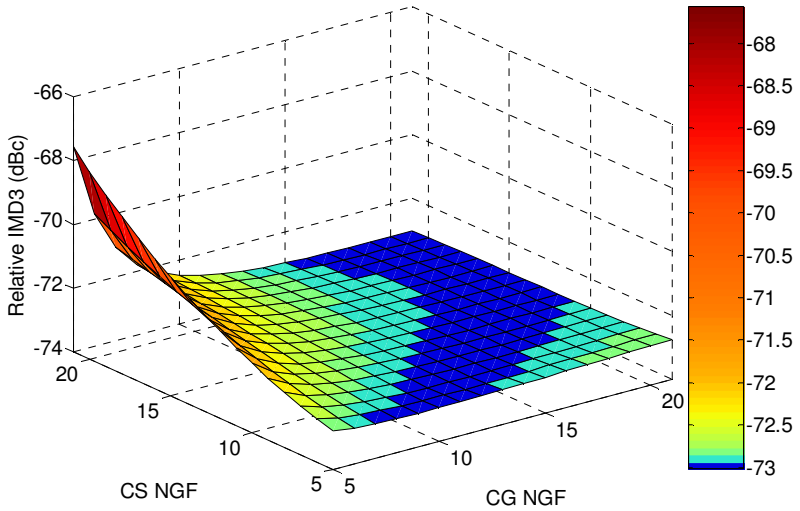
Therefore, the analysis of Figure 13 shows that the assertion in the literature [20, 21] that the CG transistor dominates nonlinear performance is only partially valid at small input powers, and becomes an even weaker approximation as the input power increases.

Figures 14(a),(b) show the change of IMD3 and the IIP3 with the CS and CG transistor sizes. Note the complete opposite colour-coded mapping between these two figures which shows that there is a direct relationship between IMD3 and the IIP3 .

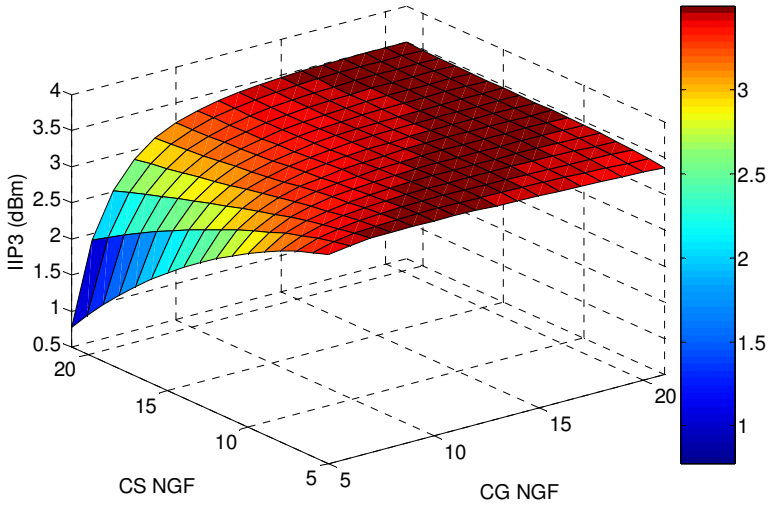
Effect of the Degeneration Inductance

The feedback provided by the degeneration inductance has two effects on the nonlinear performance of the amplifier. Since it provides negative feedback, it reduces the nonlinearity, and may lead to a smaller IMD3. However, some frequency components of that feedback contribute to increasingIMD3. For example a second-harmonic component fed back through the degeneration inductor may interact with the fundamental input through the second-order nonlinearity of the CS transistor, thus producing a new third-order intermodulation component. Therefore, careful analysis has to be conducted to evaluate the extent of these two effects on the nonlinear performance and establish if one dominates the other. ***Figure 15*** shows how the IMD3 varies with changing transistor sizes when different values of degeneration inductances are used. This analysis is carried out at 0 dBm since with this relatively high input power the nonlinearities of the circuit are manifested more than at low power operations.

An important observation from Figure 15 is that the manner of variation of IMD3 with transistor sizes does not change as the value of the degeneration inductance changes, only the value of IMD3 changes. This confirms that within a certain range of inductor values, the existence of the inductor does not change the nature of variation of RF performance parameters with respect to transistor sizes in the cascode and hence initial analysis for these performance parameters with respect to transistor sizes can safely be done without the inclusion of the degeneration inductance.



(a)



(b)

Figure 14. Mapping between IMD3 and the IIP3 calculations at -30 dBm input power versus transistor sizes: (a) IMD3and (b) IIP3.

Figure 15 also shows that as the value of the degeneration inductance increases, IMD3 decreases. This indicates that the effect of nonlinearity improvement through negative feedback exceeds the increase in IMD3 contributed by the mixing of certain feedback components with the fundamental in various orders of nonlinearity.

As expected, the degeneration inductance also affects the noise figure of the amplifier. ***Figure 16*** shows how the minimum noise figure varies with changing the transistor sizes when different values of degeneration inductances are used. Figure 16 clearly shows that the manner of variation in the minimum noise figure with respect to transistor sizes does not significantly change as the value of the degeneration inductance changes. Figure 16 also shows that the minimum obtainable noise figure will increase as the value of the degeneration inductance increases.

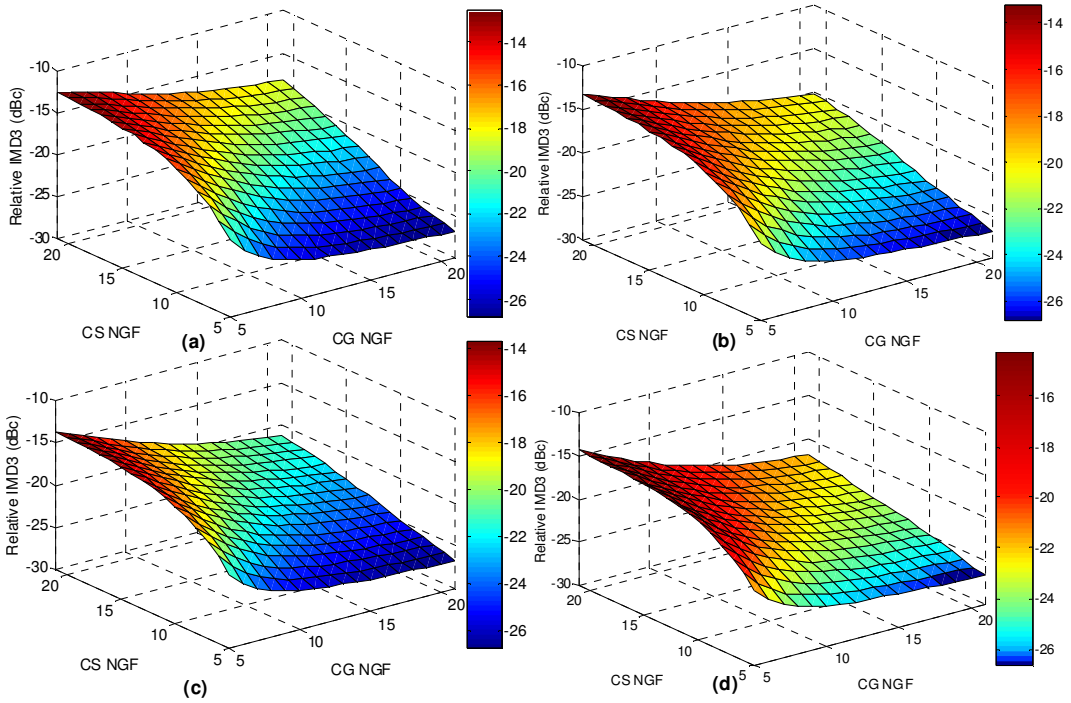


Figure 15 IMD_3 versus transistor sizes at different values of degenerating inductors (a) no degenerating inductor, (b) 0.58 nH, (c) 1.5 nH and (d) 2.9 nH.

Input power is 0 dBm in all cases.

Choice of the Load Inductor

The load inductor influences two performance parameters; the stability (because it acts as a resistive load in the output), and gain (since it is the amplifier load). The influence of the load inductor was investigated for different on-chip inductor values whilst observing the location of the stability circles and the effect on power gain. ***Figure 17*** shows how the value of the load inductor produces different stability circles at the input and output. **Table I** lists the stability regions of these circles and the maximum obtainable output power for each on-chip inductor at low and high input powers, obtained from load-pull simulations.

Figures 17(a) and (b) show how the stability situation dramatically changes when an ideal inductor (choke) is replaced by on-chip inductors; confirming that the variation is due to the series resistance of the inductors which result in resistive loading at the output. Also noticeable is the dependence of location of input and output stability circles on inductor value. Two further observations can be made from the result in Figure 17 and Table I. The first is that a higher value of load inductor does not necessarily mean increased stability as the amplifier becomes conditionally unstable at the two highest values 7 and 9 nH. The second observation is that as the value of the load inductor increases, the power gain increases. This is because the total load impedance is increased. It is worth noting that when performing this analysis, it is important to recall that increasing the on-chip inductor value increases the chip area, which is not desirable for a low cost product.

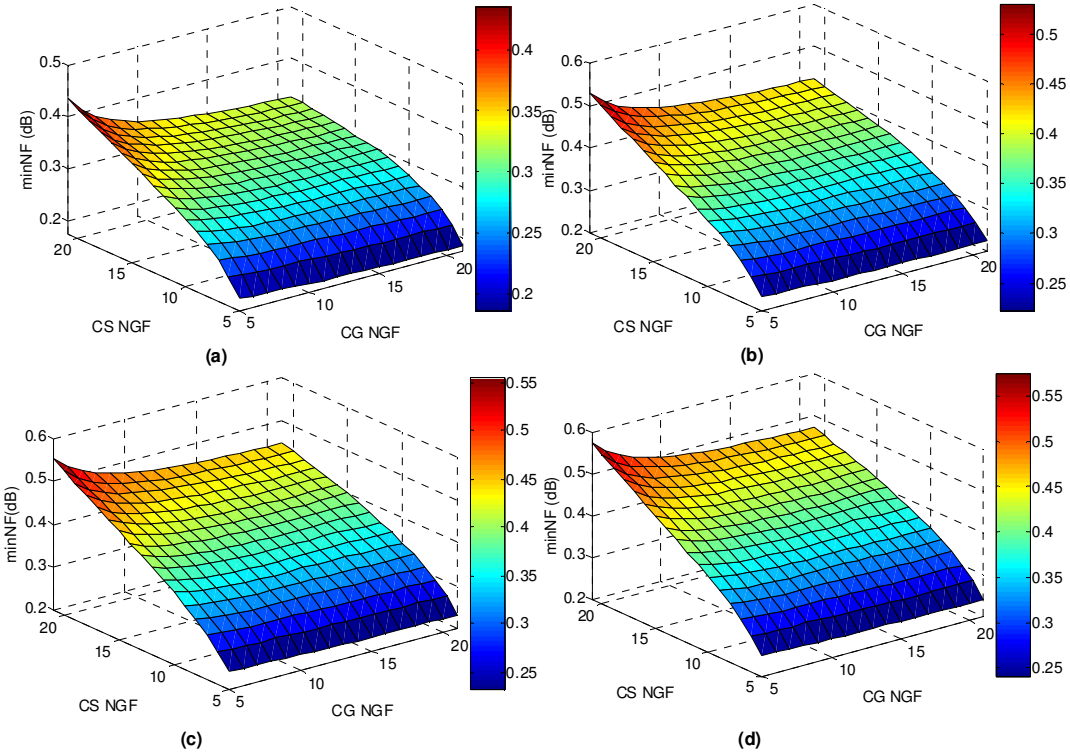
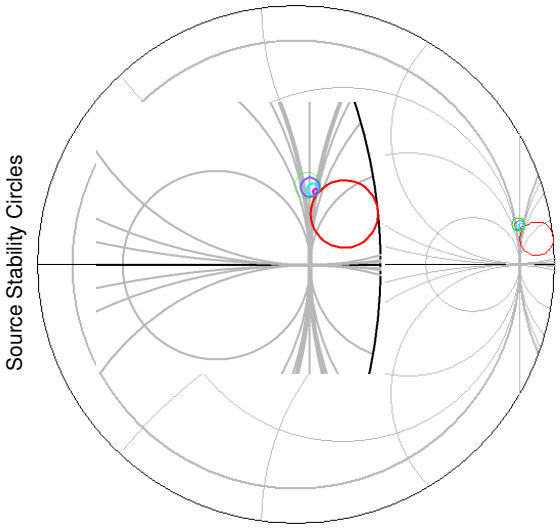
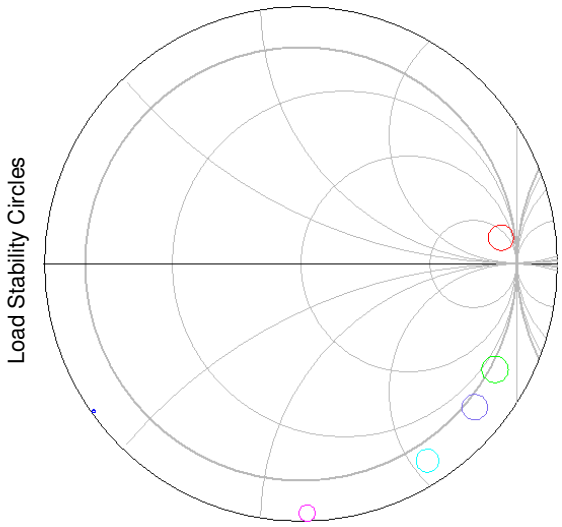


Figure 16 Minimum noise figure versus transistor sizes at different values of degeneration inductors. (a) no inductor, (b) 0.58 nH, (c) 1 nH and (d) 1.5 nH.



(a)



(b)

Figure 17. Effect of the on-chip load inductor on the stability and gain of the amplifier

Table I. Regions of stability and maximum gain relative to different load inductors

	Input Stability region	**Output stability region**	**Unconditionally stable**	**Maximum output power at -30 dBm**	**Maximum output power at 0dBm**
Choke	Inside	Outside	no	-13.7dBm	9.55dBm
1nH	Outside	Outside	yes	-24.7dBm	0.03dBm
3nH	Outside	Outside	yes	-17.5dBm	6.8dBm
5nH	Outside	Outside	yes	-15.5dBm	8.3dBm
7nH	Outside	Outside	no	-14.7dBm	8.8dBm
9nH	Outside	Outside	no	-14.4dBm	9dBm

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