Design of Source Degenerated Cascode Dual Functionality LNA/PA for the IEEE 802.15.4 (ZigBee) Standard: Part II - Example

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To illustrate the validity of the proposed design methodology, this section presents a design example for ZigBee front-end amplifier that can be used as both an LNA and a PA with acceptable performance requirements.

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Setting Up the Core Amplifier Circuit

The main DC supply voltage (connected to the drain of the CG transistor) of the proposed circuit of ***Figure 1*** is set at 1.8V which is flexible enough to allow optimisation of other circuit elements. ***Figure 2*** shows that a broad minimum in noise performance is obtained for a CS gate voltage of around 0.75V, independent of transistor size. Since the amplifier noise is strongly related to current, and there is an equal influence on current from the gate voltage and the transistor size in a CS transistor as depicted by Figure 2, the gate voltage of the CS transistor was set to 0.75V. This does not represent a constraint on any other performance parameter since full control over the DC current is still available through varying the size of the CS transistor.

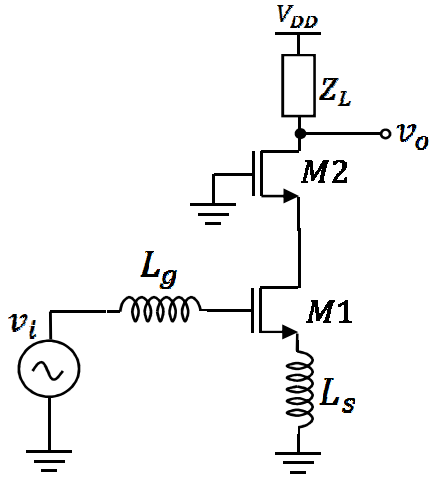


Figure 1. The common-source common-gate cascode LNA topology.

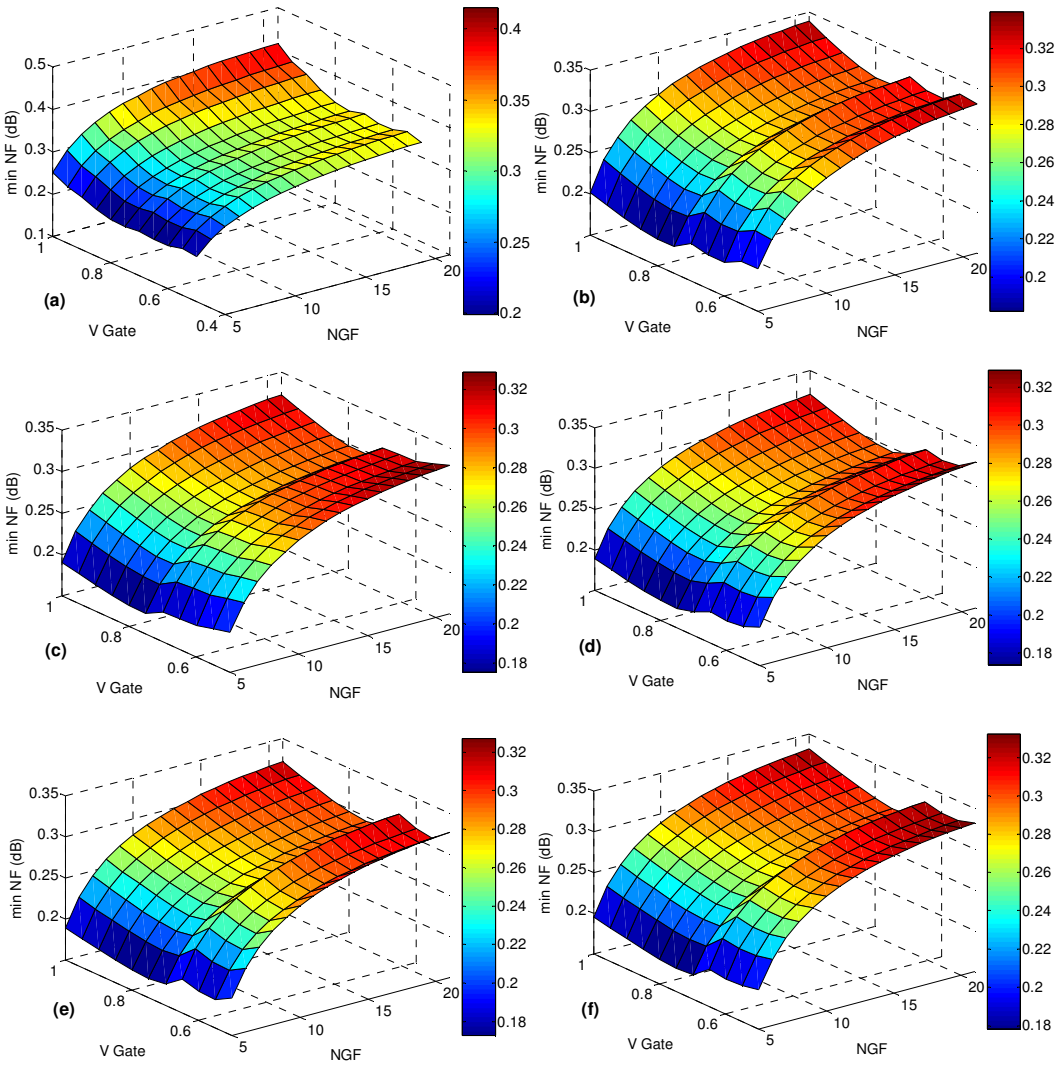


Figure 2. Minimum noise figure of a common-source transistor versus its gate voltage and size at drain voltages of:

(a) 0.3V, (b) 0.5V, (c) 0.9V, (d) 1.2V, (e) 1.5V and (f) 1.8V

Transistor sizes

The choice of transistor sizes highlights the power of the proposed design methodology; the ability to simultaneously analyse the effect of the two most important design parameters (the sizes of both transistors) on various performance parameters. Simultaneously using the results presented in the previous section and considering the required dual functionality of this amplifier, it can be concluded that, in general, a large CG transistor and a relatively smaller CS transistor will achieve a good compromise. The noise analysis in Figure 2 indicates that as the size of the CS transistor decreases,

the minimum noise figure decreases. From ***Figure 3***, the lowest IMD3 at low powers can be achieved only when the CS transistor is very small but over a wide range of large CG transistor sizes. At high power levels, the same level of minimal IMD3 can only be achieved when the CG transistor is at its maximum size as long as the CS transistor remains as small as possible.

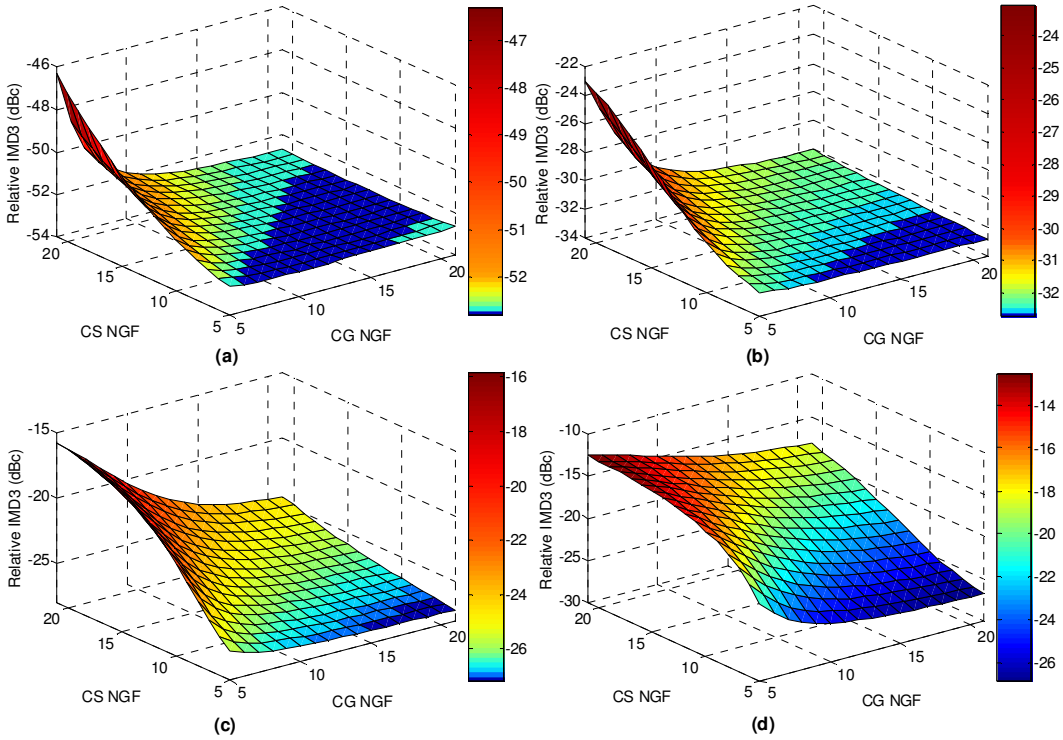


Figure 3. Variation of IMD3 in dBc with respect to transistor sizes when the RF input power is:

(a) -20 dBm (b) -10dBm (c) -5dBm (d) 0dBm

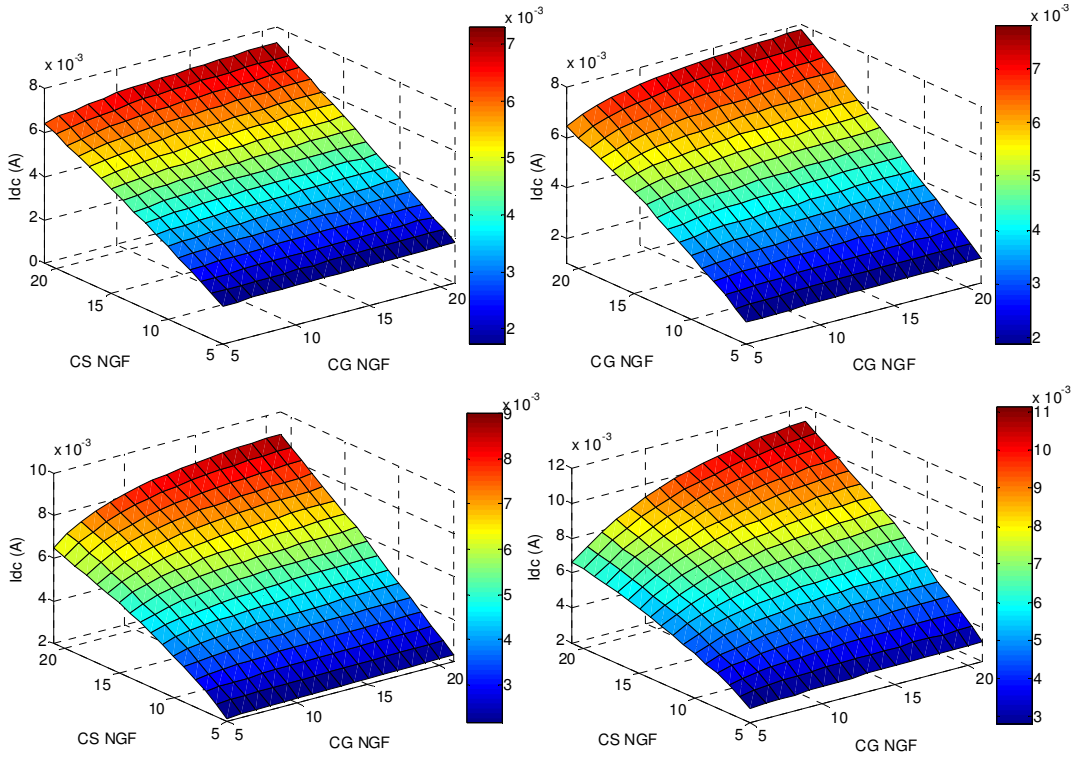


Figure 4. The DC current of the amplifier drawn from the supply at an input power of (a) -20 dBm and (b) -10 dBm (c) -5 dBm and (d) 0 dBm

Figure 4 clearly indicates that if CG transistor was to be large, the size of the CS transistor alone controls the DC current, and as a consequence, the DC power consumption, gain, delivered power, and PAE as shown in ***Figures 5-8***, respectively. ***Figures 6-8***, show that the optimum gain, power delivered to the load and PAE will result when both transistors are as large as possible but ***Figure 5*** suggests that in this case the amplifier will consume 13mW and 21mW at -20dBm and 0dBm, respectively, which are relatively high and therefore not acceptable levels of DC power consumption.

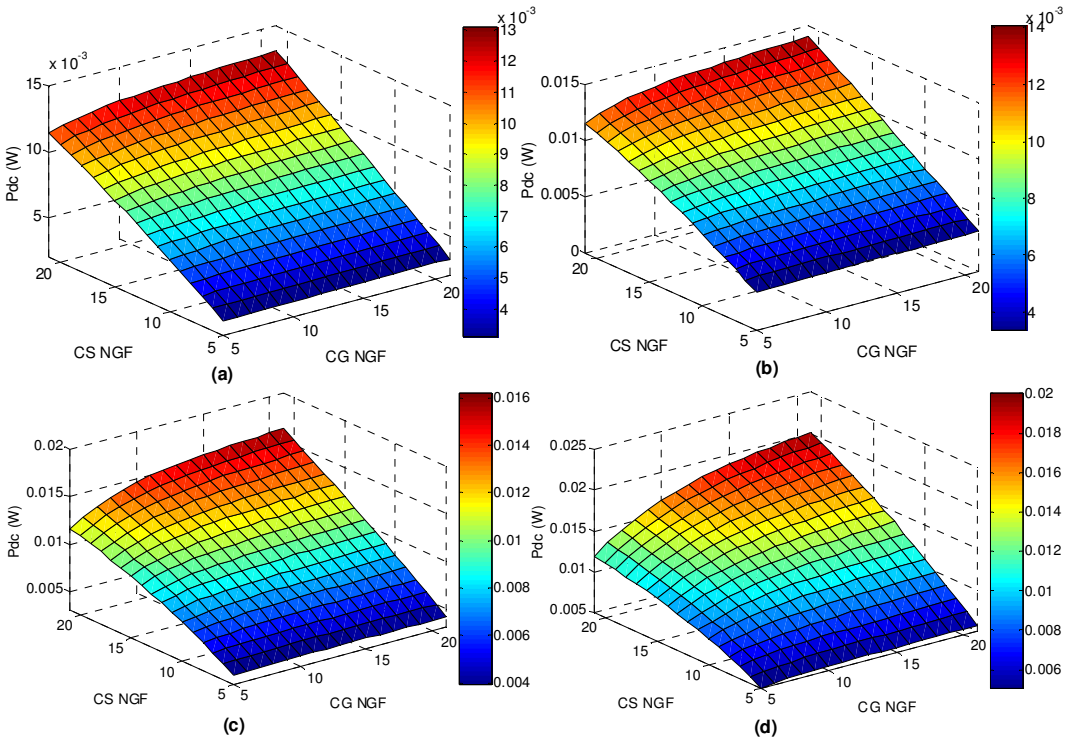


Figure 5. DC power consumption versus transistor sizes at low and high input powers (a) -20 dBm and (b) -10 dBm (c) -5 dBm and (d) 0 dBm

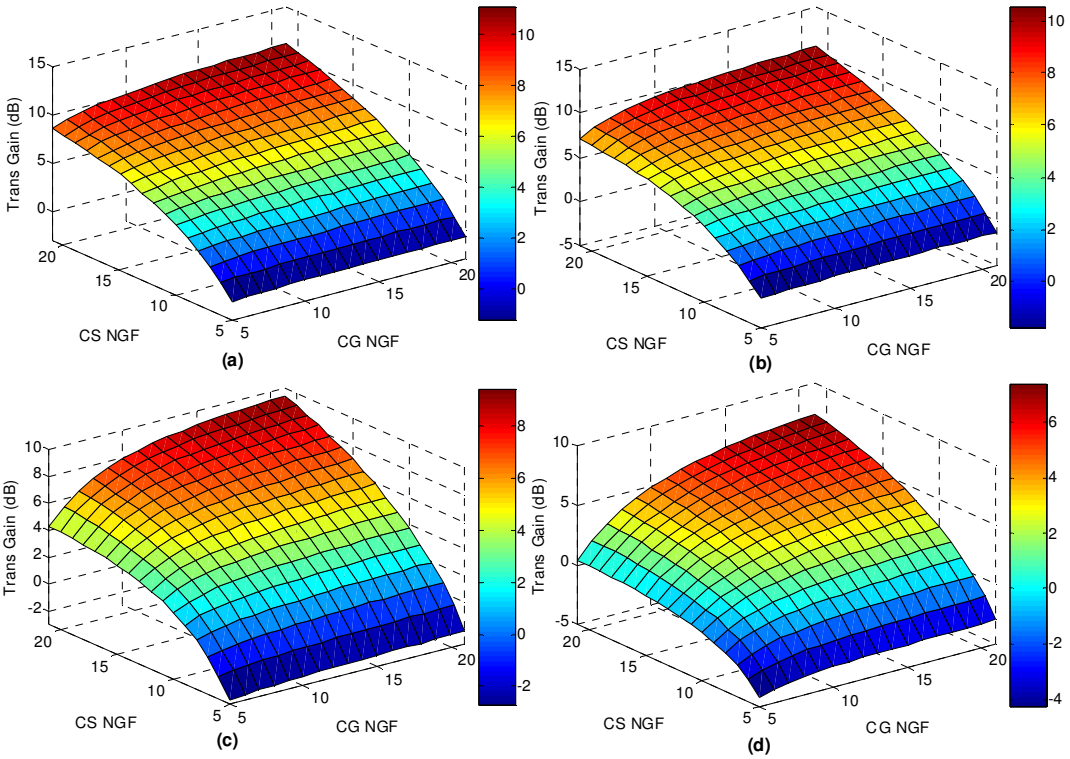


Figure 6. Transducer gain versus transistor sizes at low and high RF input powers (a) -20 dBm and (b) -10 dBm (c) -5 dBm and (d) 0 dBm

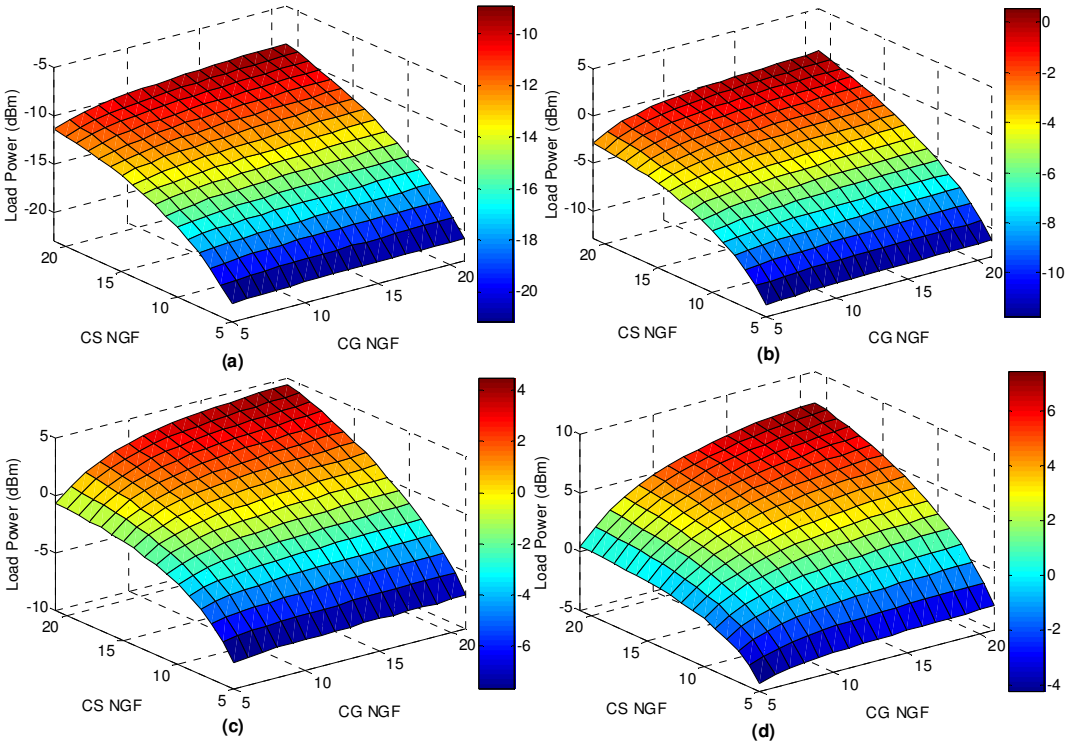


Figure 7. Load Power versus transistor sizes at low and high RF input powers:

(a) -20 dBm and (b) -10 dBm (c) -5 dBm and (d) 0 dBm

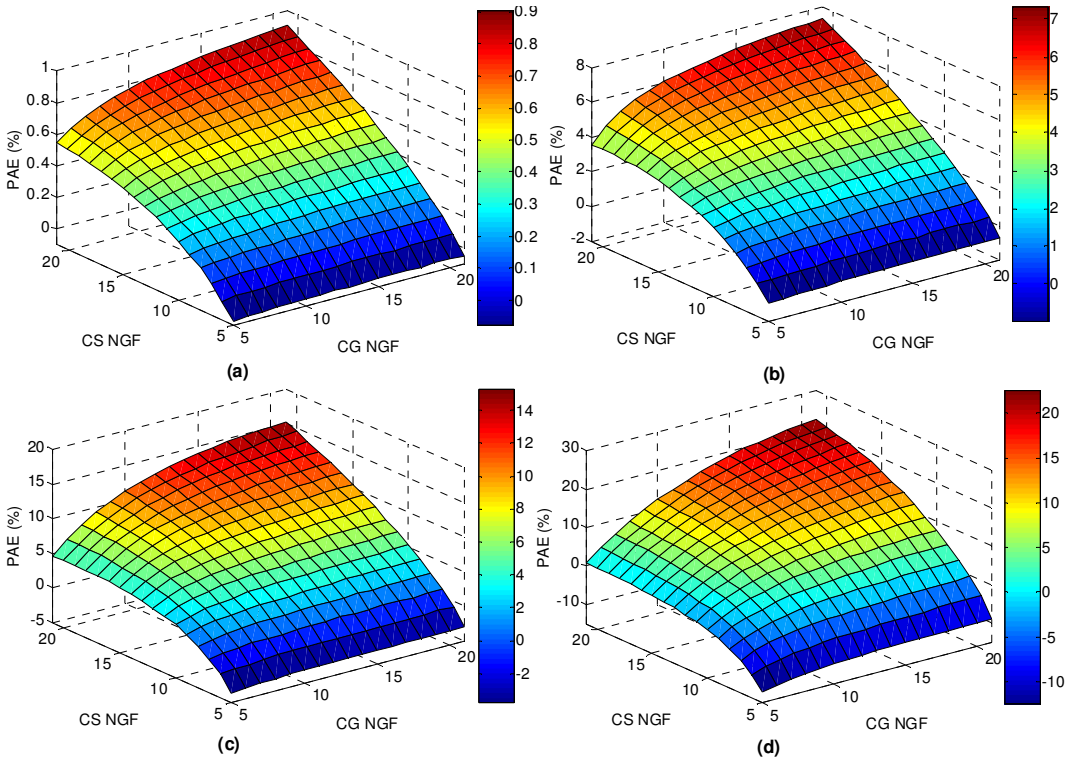


Figure 8. PAE versus transistor sizes at low and high RF input powers:

(a) -20 dBm (b) -10 dBm (c) -5 dBm (d) 0 dBm

With all dependencies simultaneously presented, designers realising amplifiers to meet varying specifications can choose transistor widths to meet their requirements. For the purpose of this example, and based on the discussion above, the number of CG transistor gate fingers is set to 20 (100µm in width) and the number of gate fingers of the CS transistor is set to 12 (60µm in width). This choice is believed to represent a good compromise between all low and high power performance parameters and satisfy the operational requirements for a LNA and a PA for a low power ZigBee front-end.

The Degeneration Inductor and the Load Inductor

According to ***Figure 9***, IMD3 decreases as the degeneration inductance increases, but the largest reduction is observed up to an inductance value of 0.58 nH, and thereafter only 1dBc improvement is obtained by increasing the inductance value to 1.5 nH. In ***Figure 10***, the minimum noise figure increases as the degeneration inductance increases, with almost equal increase between each simulated inductance value and the one below. Considering these two results and bearing in mind that noise is more of a concern at the input stage of the amplifier, a degeneration inductor of 0.58nH was chosen. With this value, a real part will be generated in the input impedance easing the choice of matching circuitry. Further, the linearity of the amplifier will be improved with only a slight increase in noise figure.

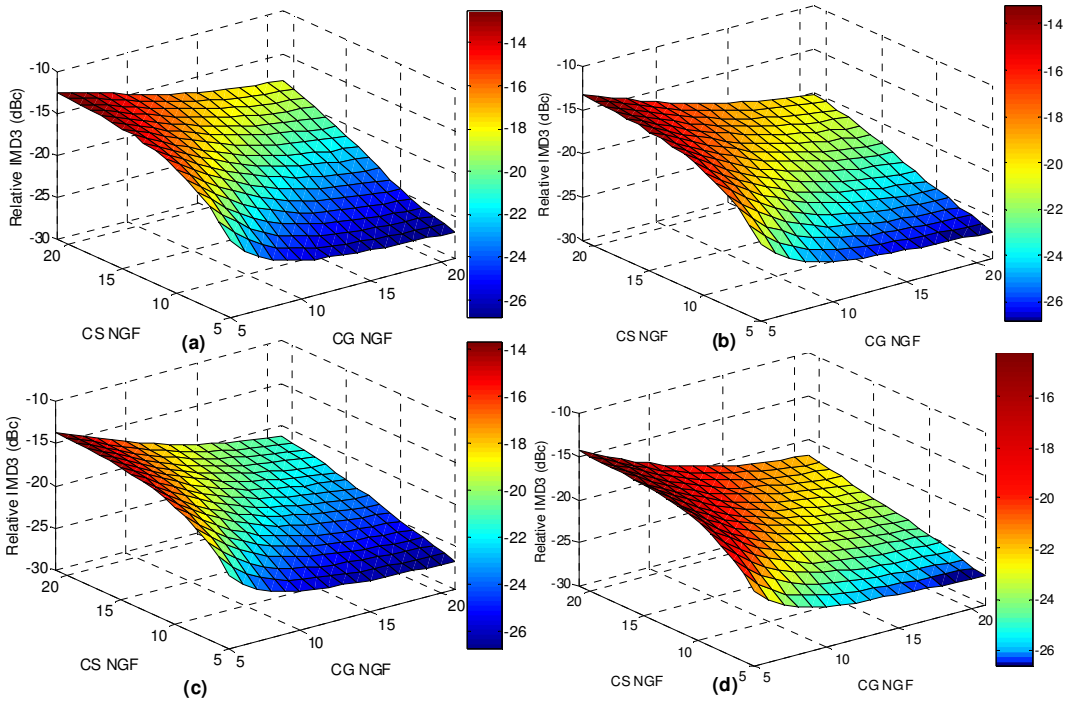


Figure 9. IMD3 versus transistor sizes at different values of degenerating inductors (a) no degenerating inductor, (b) 0.58 nH, (c) 1.5 nH and (d) 2.9 nH.

Input power is 0 dBm in all cases.

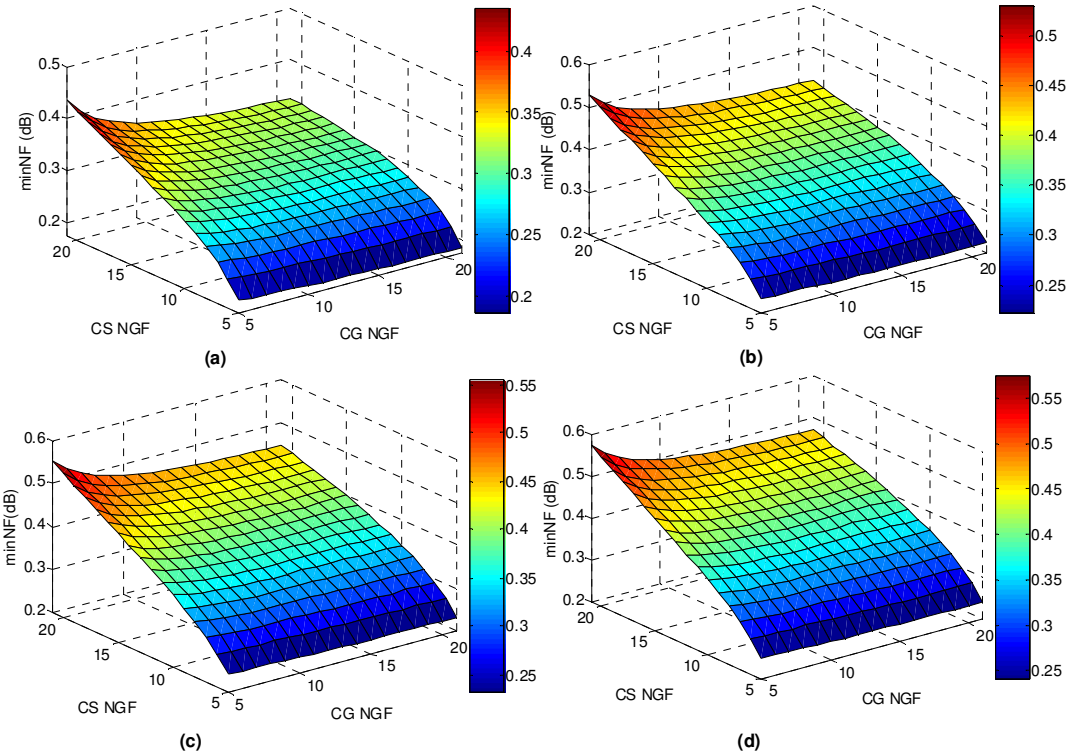
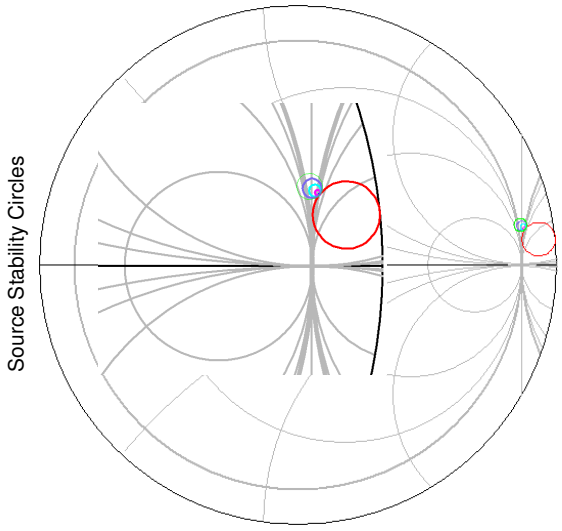
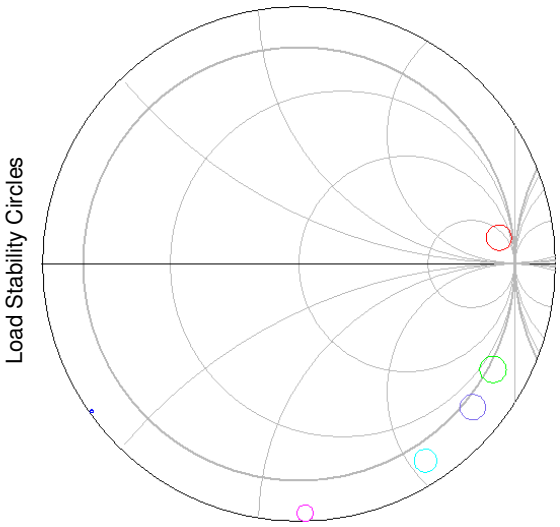


Figure 10. Minimum Noise Figure versus transistor sizes at different values of degeneration inductors. (a) no inductor (b) 0.58nH (c) 1nH and (d) 1.5nH



(a)



(b)

Figure 11. Effect of the on-chip load inductor on the stability and gain of the amplifier.

Table I. Regions of stability and maximum gain relative to different load inductors

	Input Stability region	Output stability region	Unconditionally stable	Maximum output power at -30 dBm	Maximum output power at 0dBm
Choke	Inside	Outside	no	-13.7dBm	9.55dBm
1nH	Outside	Outside	yes	-24.7dBm	0.03dBm
3nH	Outside	Outside	yes	-17.5dBm	6.8dBm
5nH	Outside	Outside	yes	-15.5dBm	8.3dBm
7nH	Outside	Outside	no	-14.7dBm	8.8dBm
9nH	Outside	Outside	no	-14.4dBm	9dBm

Based on the results reported in ***Figure 11*** and **Table I**, choosing a load inductor of 5 nH yields an appropriate trade-off between stability and power gain at both low and high powers. This value results in unconditional stability and a reasonably-sized on-chip inductor (0.05 μm^2). It also provides a good maximum output power for both low and high input power. It is important at this stage to ensure that the maximum obtainable output power is achieved, since subsequent matching to optimize other performance metrics such as PAE and IMD3 will degrade the final output power.

Linearization by MGTR

It is important to ensure that the current used in the CS transistor to improve linearity by cancelling the third-order transconductance matches the current in the CS transistor of the cascode amplifier, and also that the impact of the cascode CG transistor on the current is taken into account. These requirements can only be guaranteed by tuning the auxiliary transistors in parallel to the CS transistor while it is connected in the cascade topology. The optimisation strategy was to include three auxiliary transistors to try to achieve as wide as possible the region on the V_{GS} scale, where the third-order transconductance is zero. Because this optimisation must be performed manually, the widths of the three auxiliary transistors were set to the three smallest number of gate fingers (5, 6 and 7). With this arrangement, as well as restricting additional current drawn by the auxiliary transistors, only the gate voltages of the auxiliary transistors need be optimised, simplifying the design procedure.

Figure 12 shows the second derivative of the total transconductance of the cascode with respect V_{GS} of the CS transistor. Inspection of Figure 12 shows that, the third-order transconductance is almost zero in the range $0.68 < V_{GS} < 0.78$ V. Thus, using $V_{GS} = 0.75$ V for biasing the CS transistor would result in near zero value for the third-order transconductance. When testing the effect on linearization, a 7 dBm reduction in IMD3 was observed at low input powers in the non-matched amplifier and a 4 dBm reduction was observed with an input power of 0 dBm. This is because at low power, IMD3 comes from the third-order transconductance only, and the contribution to IMD3 from higher-order nonlinearities is negligible. As the operating power increases, the contribution of the higher-order nonlinearities becomes more significant and has to be considered.

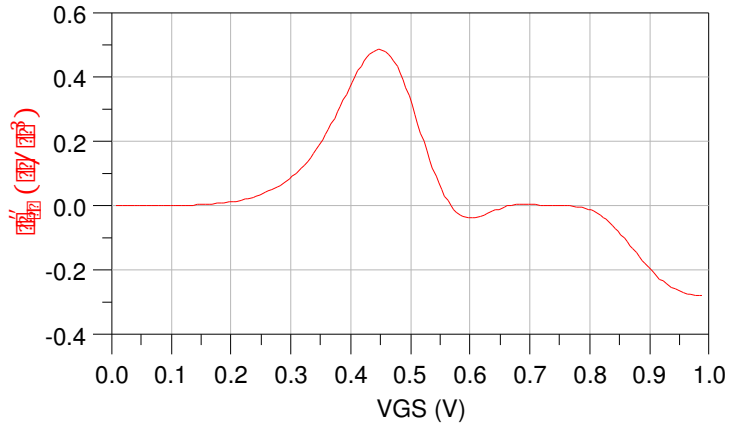


Figure 12. Second derivative (third-order transconductance) of the total transconductance in the cascode after the addition of the linearising auxiliary transistors to the CS stage.

Matching the Amplifier

Following selection of the core elements, the amplifier is matched. Matching at the input and the output will take into account the amplifier response to low and high power inputs simultaneously to make suitable tradeoffs, which guarantee an operation satisfactory to meet the requirements of both modes of operation.

Matching the input

Figure 13 shows the small signal noise circles generated from an S-parameter simulation for the input matching. Similar to stability circles, each of the noise circles represents a group of impedances which, if presented to the input of the amplifier, will yield the corresponding noise figure. It is important to note that these noise figure values are calculated in the simulator with the assumption that the output of the amplifier is conjugately matched, which is the usual practice in low power LNA design. This is not the case in this amplifier design however, since the output will be matched with respect to few other parameters (such as PAE, power delivered to the load and IMD3) due to its dual functionality requirement. Thus, the final noise figure value will be expected to change slightly. ***Figure 14*** shows the available gain circles for the core amplifier circuit generated from an S-parameter simulation. Inspection of Figures 13 and 14 shows that little trade-off is required between noise and available gain for small signal operations as the location of the optimum impedance for both are at approximately at the same location on the Smith chart.

For matching at high power operation, a source-pull simulation was performed at 0 dBm input power to generate contours indicating the relationship between the impedance presented to the input and the power delivered to the load, PAE and IMD3. These contours are presented in ***Figures 15, 16*** and ***17***, respectively. It is important to emphasise that these contours (and the contours produced for matching the output in ***Figures 19-21***) were produced by simulating as many impedance points on the Smith chart as possible, in order to increase the certainty of the results.

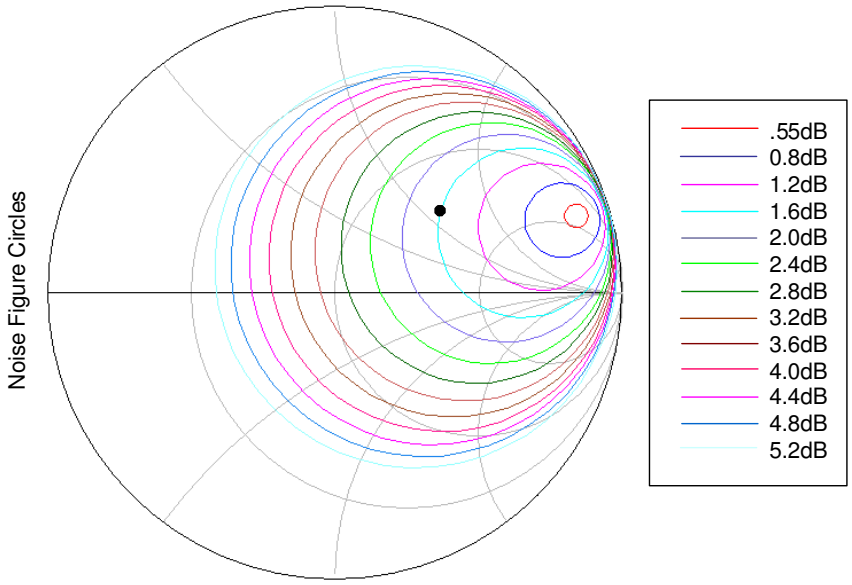


Figure 13. S-parameter noise circles for input matching (with a dark spot indicating chosen impedance)

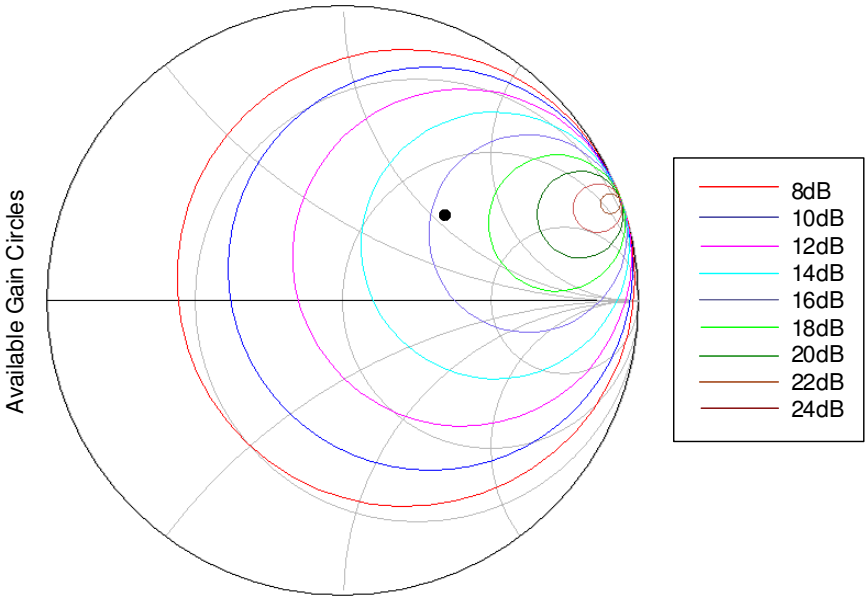


Figure 14. Available gain circles for low-power input matching (with a dark spot indicating chosen impedance)

Comparing the Figures 14, 16 and 17 reveals that little compromise is required between the power and gain characteristics for high and low power operation. However, the result in Figure 18 presents an interesting challenge. The area of the Smith chart which represents the optimum impedance for power, gain and noise requirements also represents the worst case results for IMD3. Also, in the direction where IMD3 becomes smaller, the rest of the performance parameters worsen. This represents the ultimate trade-off challenge for matching the amplifier input taking into consideration noise, gain and nonlinear performance.

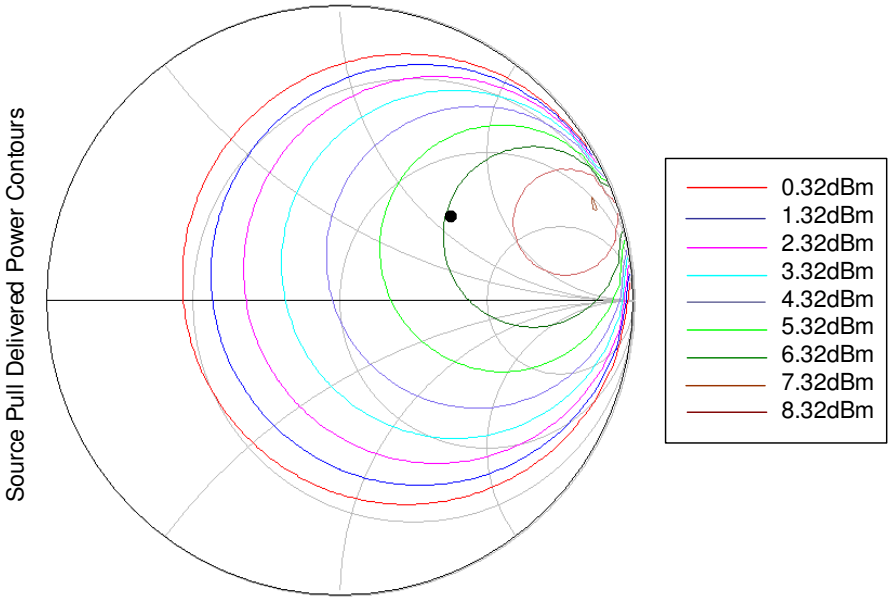


Figure 15. Power delivered to the load contours from the source-pull simulation

(with a dark spot indicating chosen impedance)

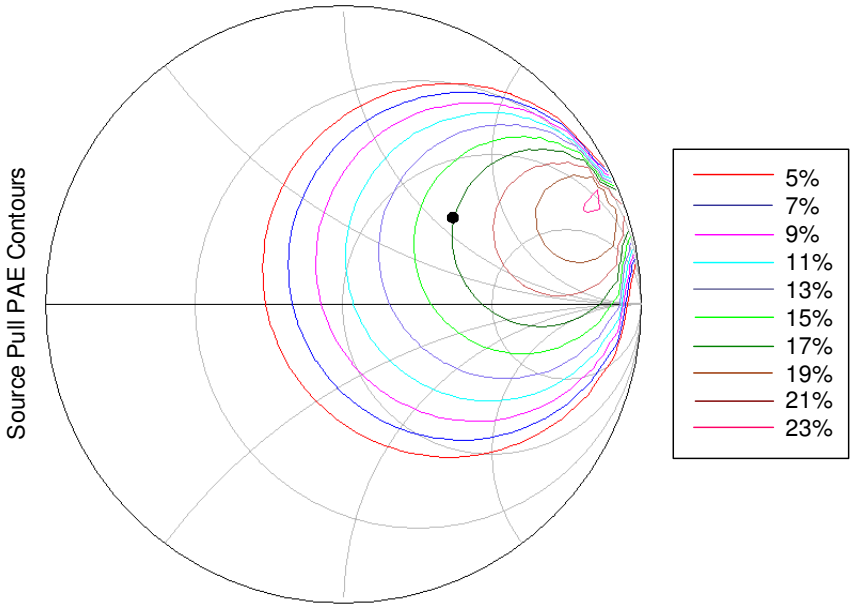


Figure 16. PAE Contours from the source-pull simulation (with a dark spot indicating chosen impedance)

Given that the noise figure is influenced by the input match much more than the output match and that the output match has a significant effect on all the other performance parameters, the input matching impedance of 84.35 + j55.75 Ω shown on each Smith chart (Figures 13-17) as a dark spot was chosen. With this impedance, the noise figure is expected to be approximately 1.6 dB and a good compromise is made between gain and linearity at the input. It is important to emphasise that these results present an initial prediction and are not final since the output matching is going to influence these performance parameters.

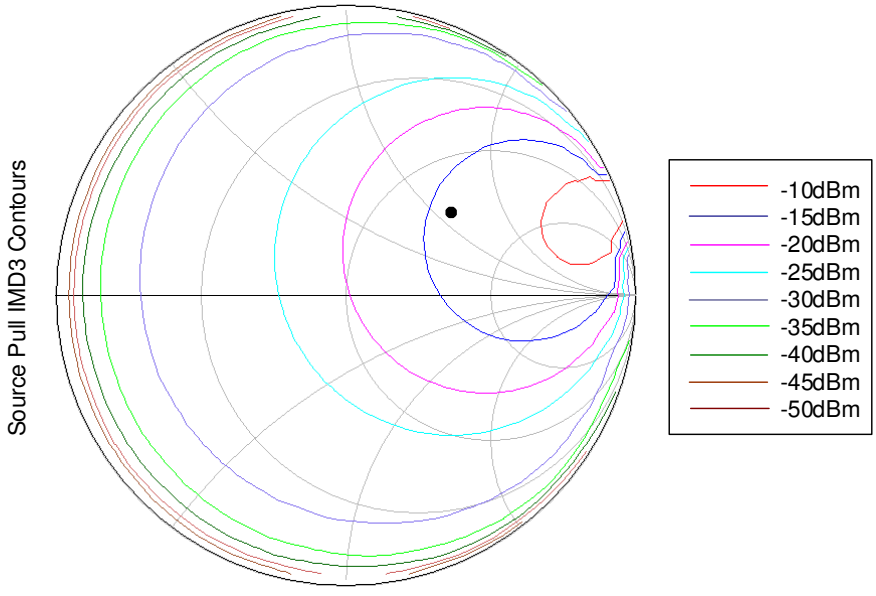


Figure 17. IMD3 contours from the source-pull simulation (with a dark spot indicating chosen impedance)

Matching the output

Matching the output of the amplifier was considered with the input matched to the impedance value mentioned above. As well as available gain, the power gain is dependent on the output matching of a network. ***Figure 18*** shows the power gain circles of the amplifier generated from an S-parameter simulation

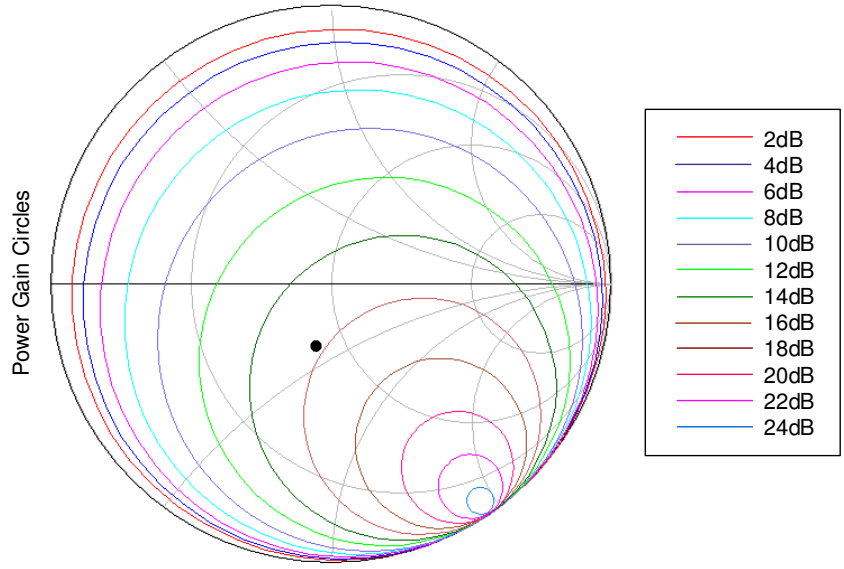


Figure 18. Power gain circles for low-power output matching (with a dark spot indicating chosen impedance)

As with the input case, a load-pull simulation at 0 dBm input power was performed at the output to investigate the matching condition for the high power operation. ***Figures 19-21*** show the generated contours for the power delivered to the load, PAE and IMD3, respectively.

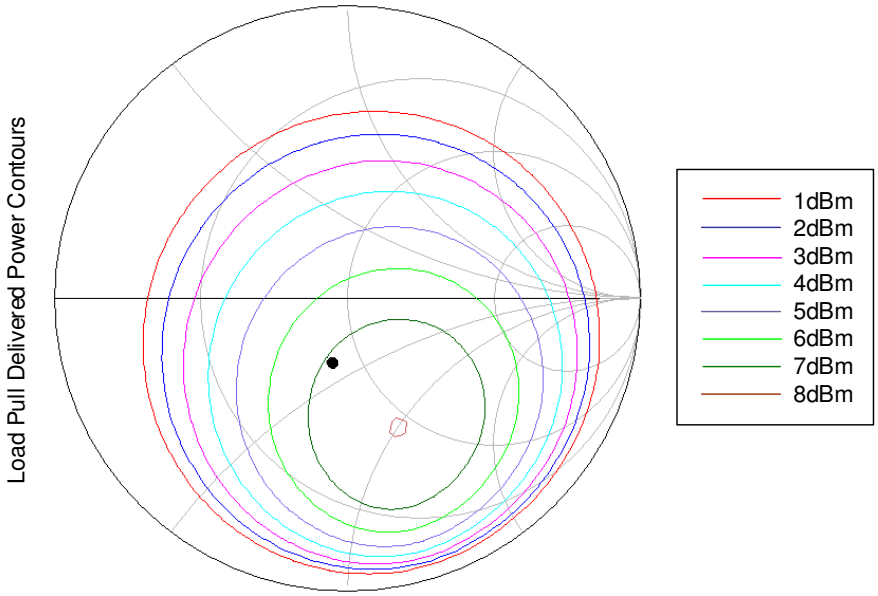


Figure 19. Power delivered to the load contours from the load-pull simulation (with a dark spot indicating chosen impedance)

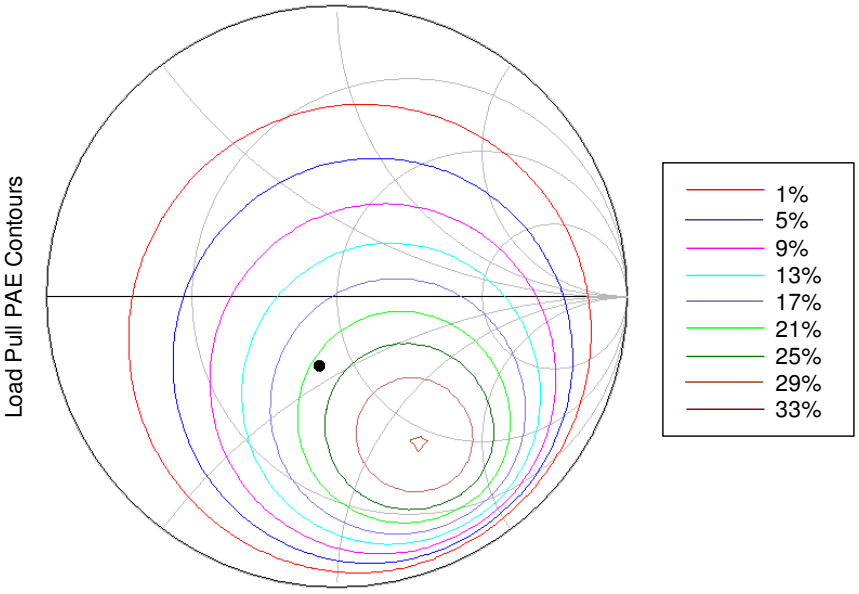


Figure 20. PAE Contours from the load-pull simulation (with a dark spot indicating chosen impedance)

Inspection of Figures 18-20 yields a similar result to that of the input match; that is little trade-off is required for output matching for gain at low and high power levels. Also similar to the situation at the input, Figure 21 shows that the ultimate trade-off is required between matching for gain and nonlinear performance at the output. This is since, again, the impedances which yield the optimum gain and delivered power performance are shown to result in the worst intermodulation performance, and vice versa.

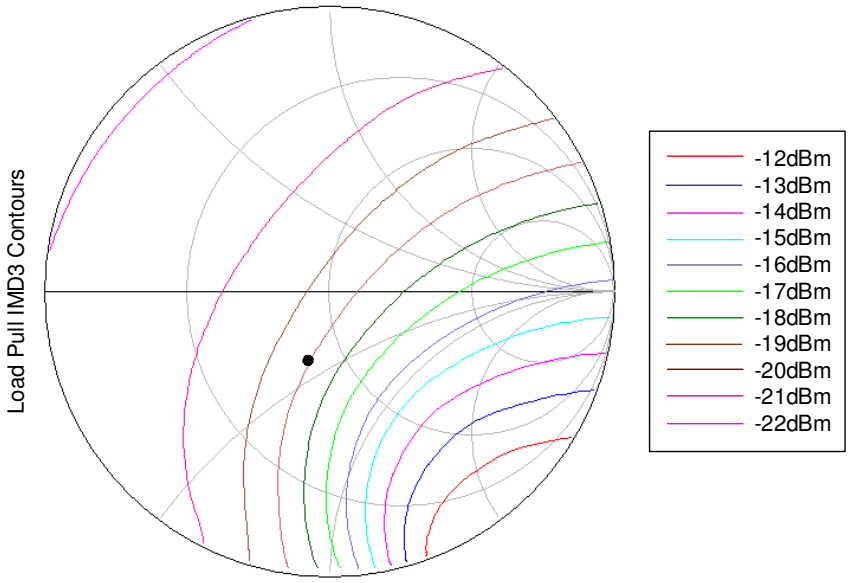
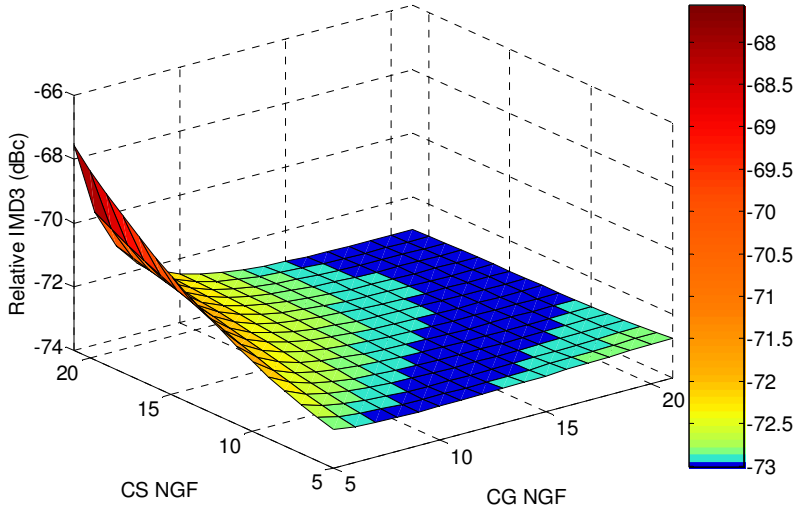
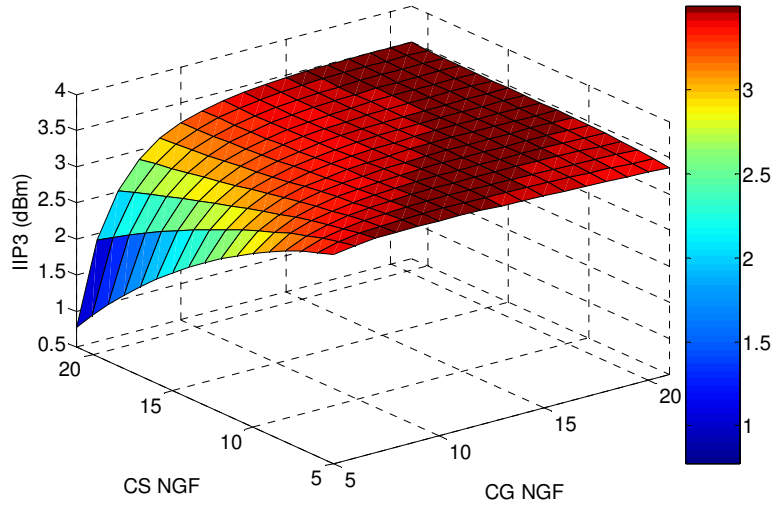


Figure 21. IMD3 contours from the load-pull simulation (with a dark spot indicating chosen impedance)

Furthermore, because the output match does not change the DC power consumption at any RF input power, then a matching impedance that is going to result in a higher PAE (at the simulated 0 dBm input power) is also going to result in a higher 1 dB compression point (as long as it is less than 0 dBm, which is normally the case). This is because a higher PAE (at the same input power and same DC power consumption) implies that more power is delivered to the load, indicating a later compression. Since there is a direct relationship between IIP3 and IMD3 as ***Figure 22*** indicates, analysing the contours in Figures 20 and 21 reveals that also a compromise need to be made between the 1dB compression point and IIP3 when considering the output match of the amplifier.



(a)



(b)

Figure 22. Mapping between IMD3 and the IIP3 calculations at -30 dBm input power (a) IMD3 and (b) IIP3, versus transistor sizes

After simultaneous consideration of the results in Figures 18 and 21, it was decided that an output matching impedance of 42.4 - j15.8 Ω will present an acceptable compromise. This point is shown on each Smith chart of Figures 18 and 21 as a dark spot.

Note that the matching impedances at the input and output were implemented with ideal lumped off-chip components from the ADS library and not using the inductors and capacitors provided in the UMC 0.18 µm design kit. This is because the quality factors of these lumped components were so high that they invalidated the designed-for matching impedances and made the matching conditions presented in Figures 14-20 practically irrelevant. This is also bearing in mind that the work being presented here emphasises more on presenting a unique and useful design methodology for LNA/PA design rather than the actual final results that can be achieved with this particular foundry design kit.

LNA/PA Performance Evaluation

This section presents the final performance results of the amplifier at low and high input powers and discusses how these satisfy the required specifications of the ZigBee front-end radio transceiver at the 2.4GHz band.

Figure 23 presents the S-parameter simulations of the matched amplifier over a range of frequencies from 1 to 4 GHz. It is shown that in the 2.40 to 2.48 GHz region (which covers ZigBee's 16 channels in this band) S_{21} is 10 dB and S_{12} is -42 dB, which presents an excellent reverse isolation at the input. However results for S_{11} and S_{22} represent a poor input and output return loss, respectively. The reason for this can be referred to the matching conditions, where the worst case compromise was required between gain and IMD3 matching.

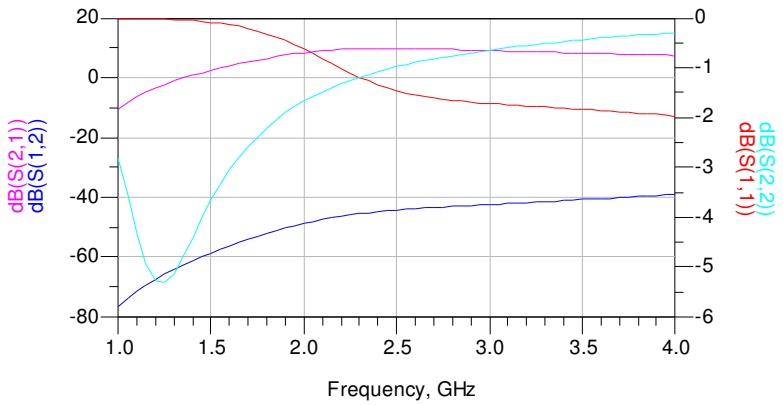


Figure 23. S-parameter simulation results of the matched amplifier

Figure 24 presents the noise performance of the amplifier over the range from 1 to 4 GHz. A minimum is observed in the band of interest between 2.4 and 2.48GHz, with a noise figure of 1.65 dB, slightly higher, as expected, than that predicted by the noise circles in Figure 13.

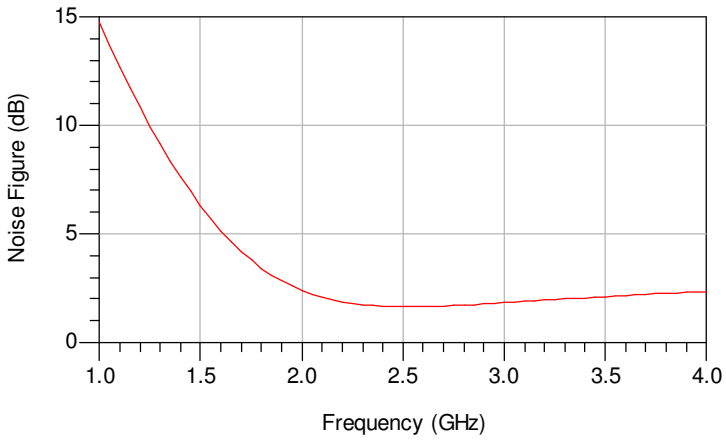


Figure 24 Noise figure vs. frequency of final amplifier

PAE and power gain results obtained from a one-tone simulation are shown in ***Figure 25***. The amplifier has its highest PAE of 20 percent when its input power is approximately 1 dBm and achieves approximately 7 dB of gain at that point. This more than satisfies the specification of the ZigBee front-end transmitter, which requires an output power of at least -3 dBm, but a higher output power is always desirable to increase the integrity of the signal and reduce the effect of interference.

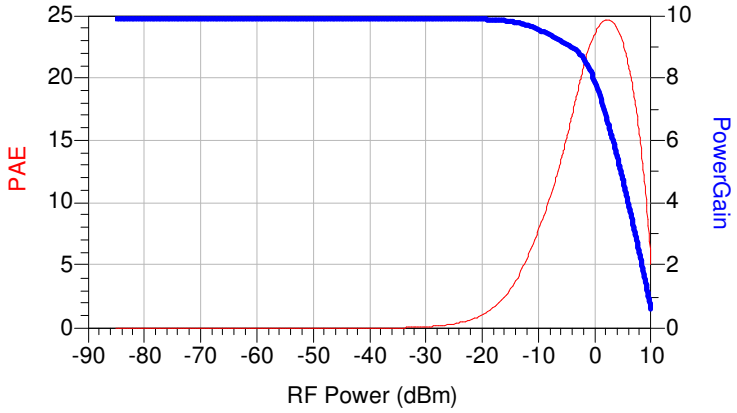


Figure 25. PAE and power gain vs. input power

Figure 26 shows how the DC current drawn from the supply, and correspondingly the DC power consumption, change as the input power changes. As expected, the DC current and DC power consumption increase as the input RF power increases. The increase starts at -25 dBm, which means it is at this value that the input RF power starts to change the DC characteristics of the amplifier. At small input powers, only 4.4 mA is withdrawn from the 1.8 V supply, yielding a DC power consumption of approximately 8 mW, which is low when compared with 14.7 mW and 11.8 mW reported in [28] and [40] . This power increases to 22 mW with only 12 mA drawn from the supply, which still represents a superior result if compared with other chips available in the market; see for example MC13191 (Freescale), AT86RF230 (Atmel), EM250 (Ember) and CC2420 (TI/Chipcon) bearing in mind that the power amplifier consumes most of the power in a transmitter. Note how the DC power consumption of the final design agrees with that predicted by the initial optimisation study of Figure 5 (despite the slight increase due to the current in the auxiliary transistors added for linearization).

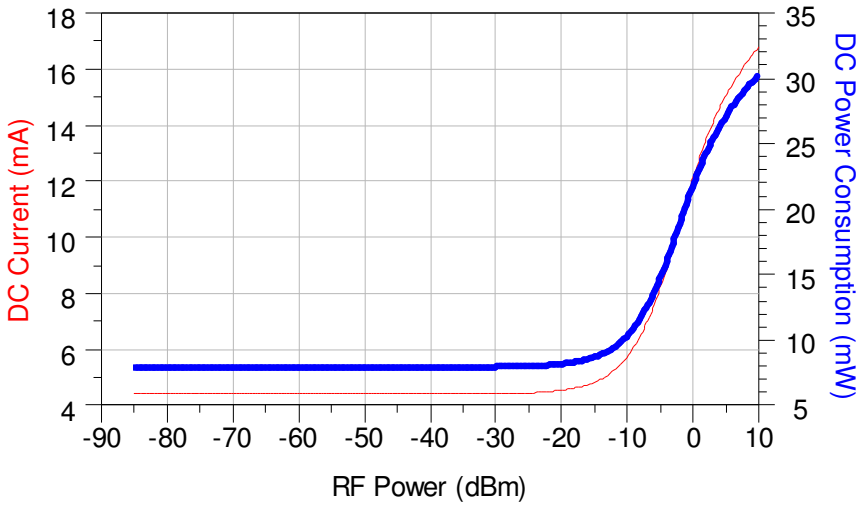


Figure 26. DC current and DC power consumption vs. input RF power

Figure 27, shows the results obtained from a one tone simulation to determine the 1 dB compression point. It appears that the amplifier compresses at approximately -3.5 dBm input power. ***Figure 28*** presents the result of a two tone simulation showing that the amplifier achieves an IIP3 of 6 dBm.

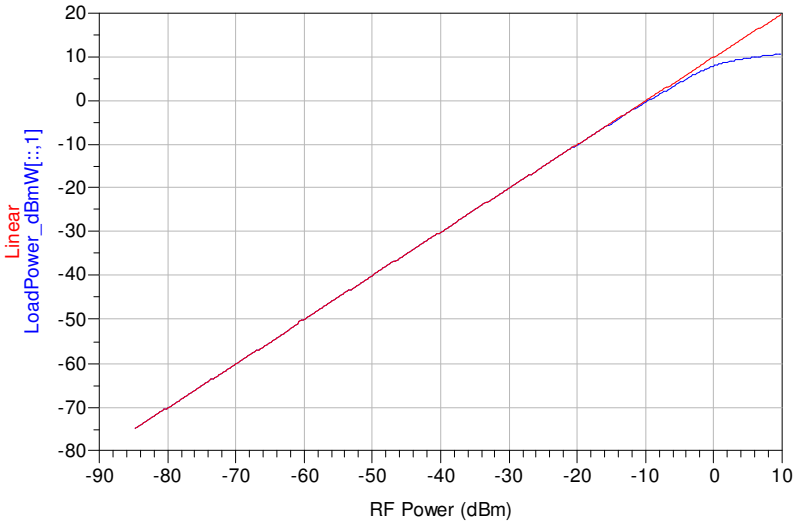


Figure 27. One-tone harmonic balance simulation results of the matched amplifier

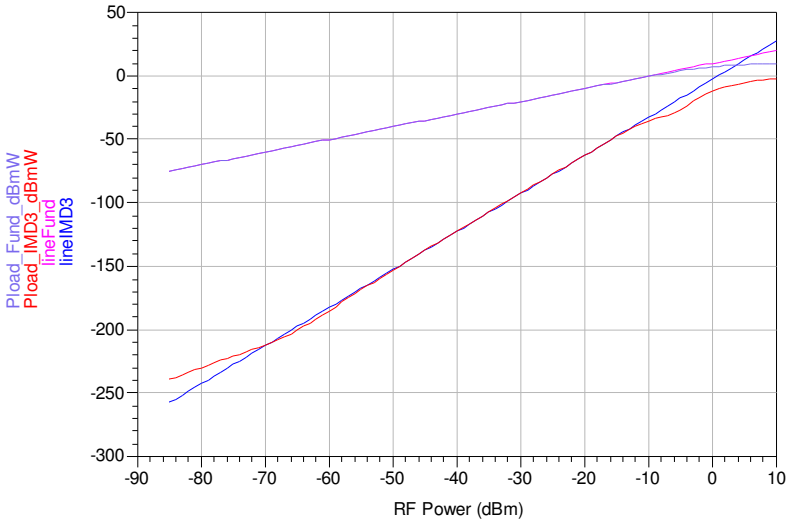


Figure 28. Two-tone harmonic-balance simulation results of the matched amplifier

Obtaining the results above involved no ambiguous automatic optimisation in the simulator and did not require any iteration at the end of the design flow. Optimising the core transistor circuit and the matching was based entirely on visual analysis. This demonstrates the significance of the proposed design methodology, which enabled the exploration of the available space of possibilities in the design and allowed the designer to make efficient trade-off choices, making this design possible.

It is not possible to directly relate the results obtained from the designed amplifier with LNA requirements of the ZigBee standard in the receiver. This is because the standard does not provide specifications for particular circuits in the receiver but for the receiver as a whole. For example, the sensitivity is defined as the lowest input power the receiver can detect while achieving a Packet Error Rate (PER) below a pre-specified maximum. PER is defined as the ratio of error in received packets when compared with the transmitted packets. Therefore, in order to quantify PER, the received signal has to be demodulated and processed in baseband before the received packets can be compared with the transmitted packets. In another example, the 30 dB requirement for alternate channel rejection means that the adjacent channel should be attenuated by a factor of 1000. This is usually achieved through a combination of several filtering and mixing stages in the receiver beyond the LNA.

Therefore, in order to asses the designed amplifier for the LNA requirements of ZigBee, its performance is compared with the LNA sections of recently published 2.4 GHz full ZigBee transceiver designs. The performance parameters of concern are noise figure, gain, reverse isolation, input and output return loss, IIP3 and 1dB compression point, where LNA-only data is available.

This difficulty in assessing the compatibility of the amplifier with the requirements of the standard does not apply to the PA. This is because the PA is the last element in the transmitter path, and hence its compatibility to the standard can be assessed with reference to the transmitter's output specifications.

Table II presents a summary of the results of the designed amplifier and comparison with other ZigBee front-end designs. Both LNA and PA comparison is

undertaken on worst case basis. The idea is, if the designed amplifier in this work can perform better than the worst published ZigBee-compatible design, then it must also be ZigBee-compatible.

Table II Amplifier results comparison with ZigBee-compatible LNA and PA

Comparison Parameter	**This work**	**Worst case value**	**Reported in**
IIP_3 (dBm)	6	-9	[59]
1dBc (dBm)	-3	-21	[60]
LNA			
Gain (dB)	10	10	[41]
Reverse Isolation (dB)	-42	-28	[59]
Input return loss (dB)	-1	-17	[61]
Output return loss (dB)	-1	-12	[62]
Power Consumption (mW)	7.2	5.4	[63]
NF (dB)	1.6	4.9	[59]
PA			
Maximum Output power (dBm)	10	0	[62]
Power Consumption (mW)	22@6dBm output	26@6dBm output	[60]
PAE (mW)	25%@6dBm output	15% @6dBm output	[60]

Due to its dual functionality target, there are no grounds of comparison between the amplifier designed in this work and LNA-only or PA-only designs. However, what is important is that the designed amplifier achieves acceptable performance satisfying each functionality, subject to the ZigBee requirements. Table II shows that the results obtained for this amplifier design in both low noise and power amplifier operations are inline with the requirements of ZigBee. This is with the exception of the input and output return losses, which are clearly significantly much higher than those of other designs. Although reverse isolation is very high and ZigBee does not have any specifications for input and output return loss, this may still cause problems due to the reflected power back to the antenna. As explained earlier, this result was due to the required trade-off in matching the input and output which appeared to have the worst case possible. A possible solution to this problem is to find the location of the contours on the Smith chart as a function of the sizes and biases of the transistors in the core amplifier circuit and to involve these contours in the trade-off decisions taken in designing these components.

Conclusion

In this article, a design methodology has been presented for a dual functionality LNA/PA. The proposed design methodology started by selecting the CS-CG cascode topology as the most appropriate for providing independent control for the linearity and

noise performance. The design methodology was then introduced by first laying out the major steps of the design flow and then implementing these steps individually. The design methodology was based on simultaneous visual analysis of the effect of variations in various core amplifier components on low and high power performance of the selected cascode topology, with focus on the sizes of the CS and CG transistor stages. A design example then demonstrated the effectiveness and usefulness of the proposed design methodology in designing an amplifier whose performance is sufficient for the requirements of both an LNA and PA of the ZigBee standard. The proposed LNA/PA uses only the basic cascode topology in addition to some low power linearization techniques and achieves excellent performance compared with recently published designs.

The major advantage of the proposed design methodology is that it facilitates the simultaneous analysis of several performance parameters with respect to the two most influential components in the architecture; the CS and the CG transistors. Simultaneously analysing both transistors and considering their common current, the representation was based on visual observation, in 3D graphs, of how performance parameters vary with related design parameters. Taking into account the multiple dependencies of performance parameters on design parameters, enables the designer to make satisfactory trade-off decisions. Components were simulated between their minimum and maximum values to explore their full potential and uncover areas of their operation where better results may be obtained, overcoming the weaknesses of mathematical equation-based approaches where this is not possible. The proposed design methodology also gives the designer the ability to reuse the results of this analysis and change trade-off choices if another design with different constraints was needed.

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